



B75H2-AM-DNI

Rev :A

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NOTE:

Design by
473718 Maho Bay and Carlow-WS Platforms - Design Guide - Rev. 1.5,
474146 Panther Point_EDS_Rev1.5
MahoBay_CRB_Rev0.7

REVISION HISTORY:

Rev	Date	Notes
V.A	2012/01/02	Initial version

Table 1-2. Desktop Panther Point Chipset SKUs

Feature Set	SKU Name					
	Q77	Q75	B75	Z77	Z75	H77
PCI Express* 2.0 Ports	8	8	8	8	8	8
PCI Interface	Yes	Yes	Yes	No ³	No ³	No ³
Total number of USB ports	14	14	12 ⁴	14	14	14
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4	4	4	4	4	4
• USB 2.0 Only Ports	10	10	8	10	10	10
Total number of SATA ports	6	6	6	6	6	6
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁵	1 ⁶	1 ⁶	2 ⁵	2 ⁵	2 ⁵
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4
HDMI/DVI/VGA/DisplayPort*/eDP*	Yes	Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	Yes ⁷	No	Yes	Yes
	Intel® Smart Response Technology	Yes	No	No	Yes	No
Intel® Anti-Theft Technology	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 8.0	Yes	No	No	No	No	No
Intel Fast Flash Standby ⁸	Yes	No	No	No	No	No

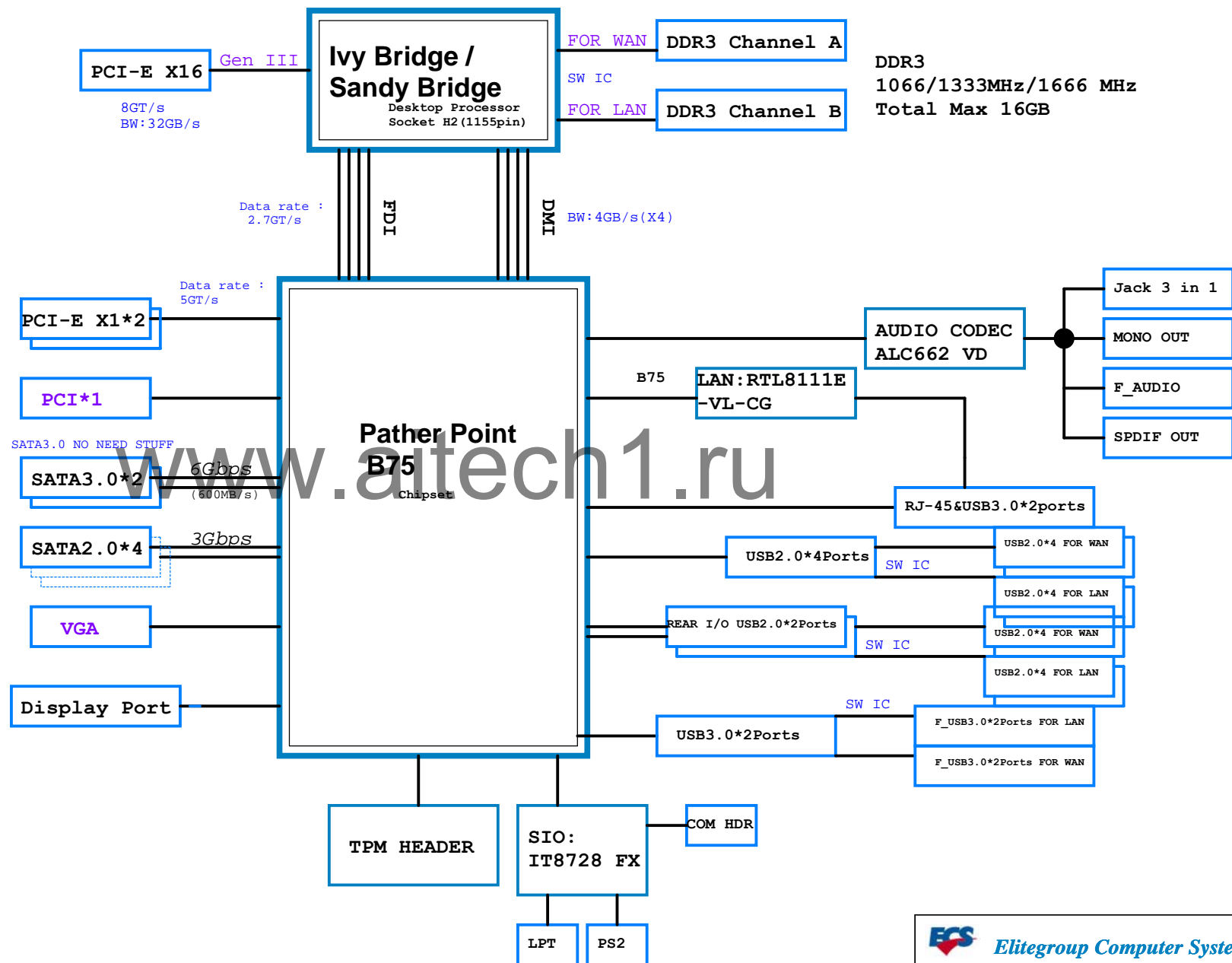
NOTES:

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.1.9 for more details.
4. USB ports 6 and 7 are disabled.
5. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
6. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
7. Supports RAID 1 only.
8. Intel Fast Flash Standby naming is not final at this time and is subject to change.



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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	OBR	GPI
GPIO6	VCC4	Over_temp	GPI
GPIO12	3VSB	LAN_DISABLE_L	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	OE_L DETECT	GPI
GPIO27	SB_3VSB	DEEP LANWAKEB	GPI
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP0_L	GPI
GPIO59	3VSB	LAN_LED_D	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	F_USB3 Power Control	GPO
GPIO44	3VSB	FOR ACER GPIO	GPI
GPIO46	3VSB	FOR ACER GPIO	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO14		Over_temp	
GPIO34		MB_ID1	
GPIO16		SIO_BEEP	
GPIO22		SIO_LED1	
GPIO23		SIO_LED0	
GPIO35		MB_ID2	
GPIO36		NET_SEL	
GPIO40		5VDAUL_MEM Control	
GPIO64		MODE_SEL	
GPIO47		TP_VGA	
GPIO41		SEL1 DETECT	

Straping Table

FCH Straping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

No Reboot:

FCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

SIO IT8728F D/EX/FX Straping (Page.26)

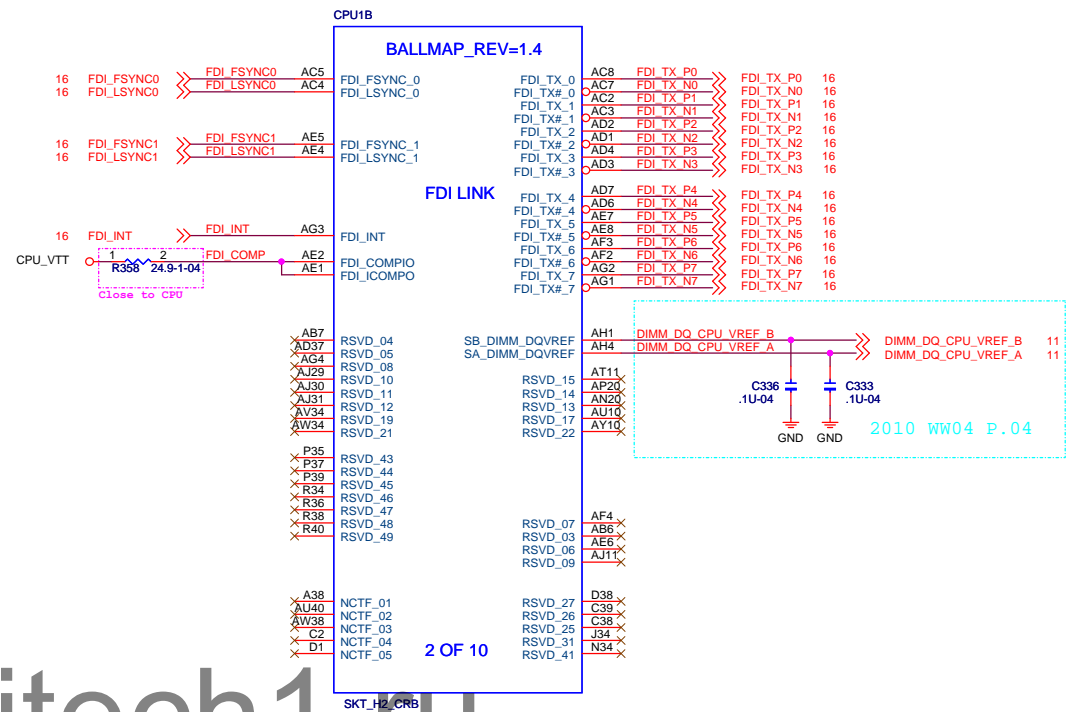
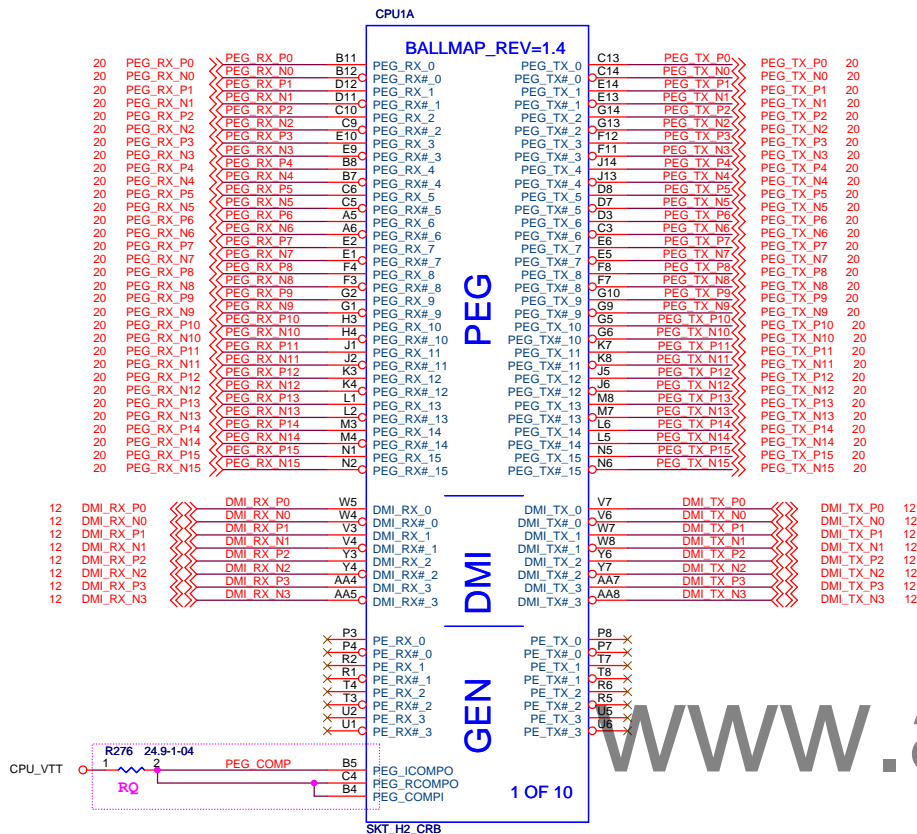
Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-48		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-29	OV/UV	0	Force Mode

* Port 1 or Port 9 is USB 2.0 Debug Port

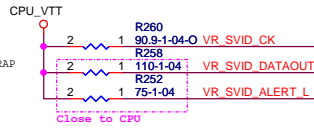
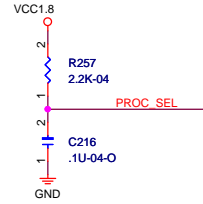
Panther point INT# Table

Function	INT Port	PCI-EX1 Port	Chip
Lan Ethernet Controller	INTC# (Default)	Port3	Intel 82579LM / Realtek RTL8111E
SATA 1&2 Controller (IDE Mode)	INTB# (Default)	NA	PCH intergrated
PCIEX Slot	INTD# (Default)	Port4	External PCIEX Card



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ. 1
 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

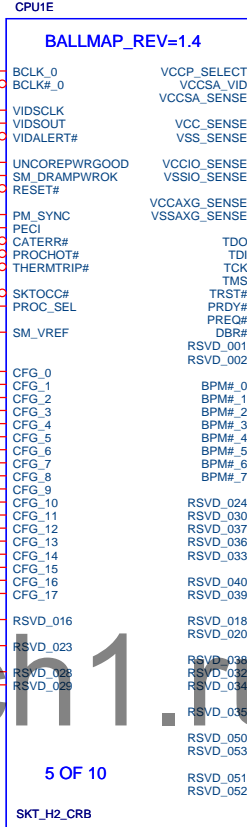


40 VR_SVID_CK
40 VR_SVID_DATAOUT
40 VR_SVID_ALERT_L

15 CK_CPU_100M_P
15 CK_CPU_100M_N
13 PM_SYNC
26 H_PECI
13 CPU_THERMTRIP_L
14,40 H_SKT0CC_L
16 PROC_SEL

CK CPU 100M P
CK CPU 100M N
VIDCLK
VIDSOUT
VIDALERT#
CPU PWROK RC
DRAM PWROK RC
CPU RST L RC
PM_SYNC
H_PECI
CATERR#
PROCHOT#
THERMTRIP#
H_SKT0CC_L
PROC_SEL
DIMM VREF CPU

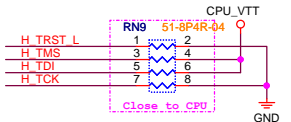
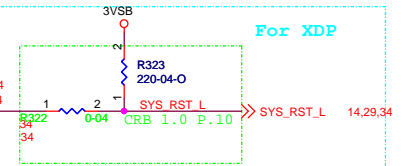
W2
W1
C37
B37
A37
J40
AJ19
F36
E38
J35
H34
G35
AJ33
K32
AJ22



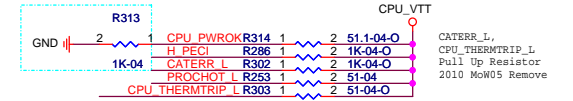
BCLK_0
BCLK#_0
VCCP_SELECT
VCCSA_VID
VCCSA_SENSE
VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSSIO_SENSE
VCCXAG_SENSE
VSSXAG_SENSE
TDO
TDI
TCK
TMS
TRST#
PRDY#
PREQ#
DBR#
RSVD_001
RSVD_002
BPM#_0
BPM#_1
BPM#_2
BPM#_3
BPM#_4
BPM#_5
BPM#_6
BPM#_7
RSVD_024
RSVD_030
RSVD_037
RSVD_036
RSVD_033
RSVD_040
RSVD_039
RSVD_018
RSVD_020
RSVD_038
RSVD_032
RSVD_034
RSVD_035
RSVD_050
RSVD_053
RSVD_051
RSVD_052

P33 VTT_SEL
P34 VCCSA_VID
T2 VCCSA_SENSE
A36 VCC_SENSE
B36 VSS_SENSE
AB4 VCCIO_SENSE
AB3 VSSIO_SENSE
L32 VCCXAG_SENSE
M32 VSSXAG_SENSE
L39 H_TDO
M40 H_TDI
M40 H_TCK
L38 H_TMS
J39 H_TRST_L
K38 H_PRDY_L
K40 H_PREQ_L
E39 H_DBR
C40 XDP_H_CLK_DP
D40 XDP_H_CLK_DN

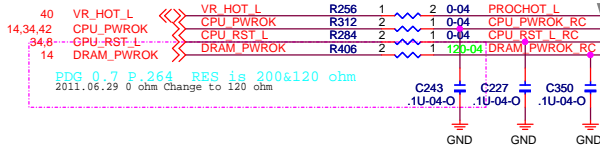
38 VTT_SEL
38 VCCSA_SENSE
40 VCCSA_SENSE
40 VCC_SENSE
40 VSS_SENSE
39 VCCIO_SENSE
39 VSSIO_SENSE
40 VCCXAG_SENSE
40 VSSXAG_SENSE
34 H_TDO
34 H_TDI
34 H_TCK
34 H_TMS
34 H_TRST_L
34 H_PRDY_L
34 H_PREQ_L
34 H_DBR
34 XDP_H_CLK_DP
34 XDP_H_CLK_DN



CBR 1.0 P.10

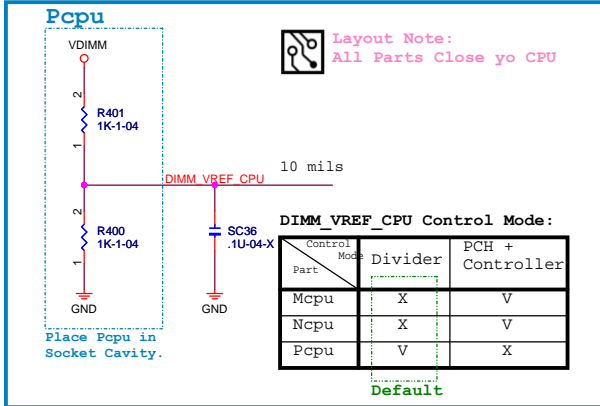


34 CFG_0 << CFG_0
To Hook2 for PDG Require



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2011.09.10 Remove Divider Control Circuit



DIMM_VREF_CPU Control Circuit

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0] X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG [0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

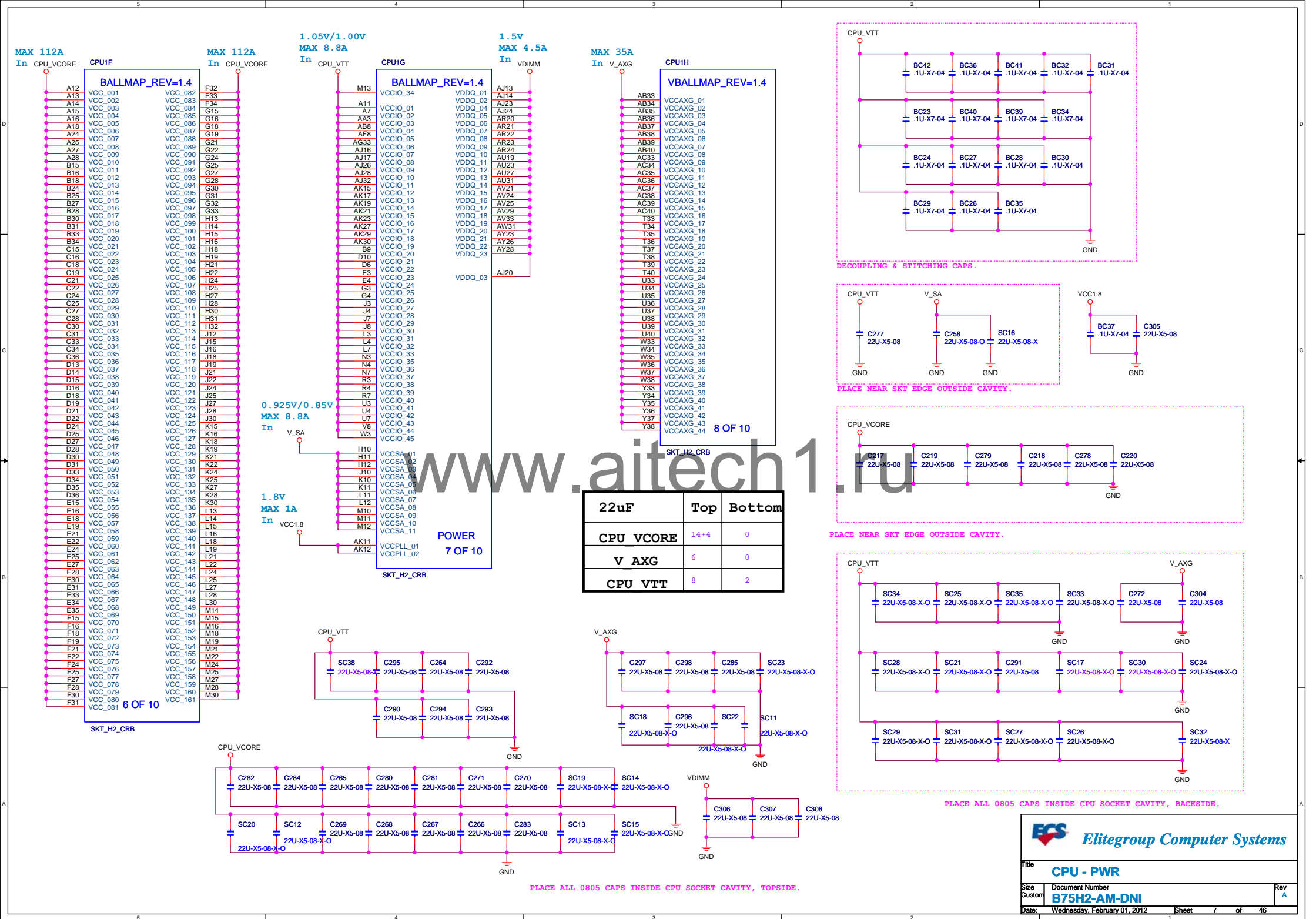
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

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Title: **CPU - MISC**

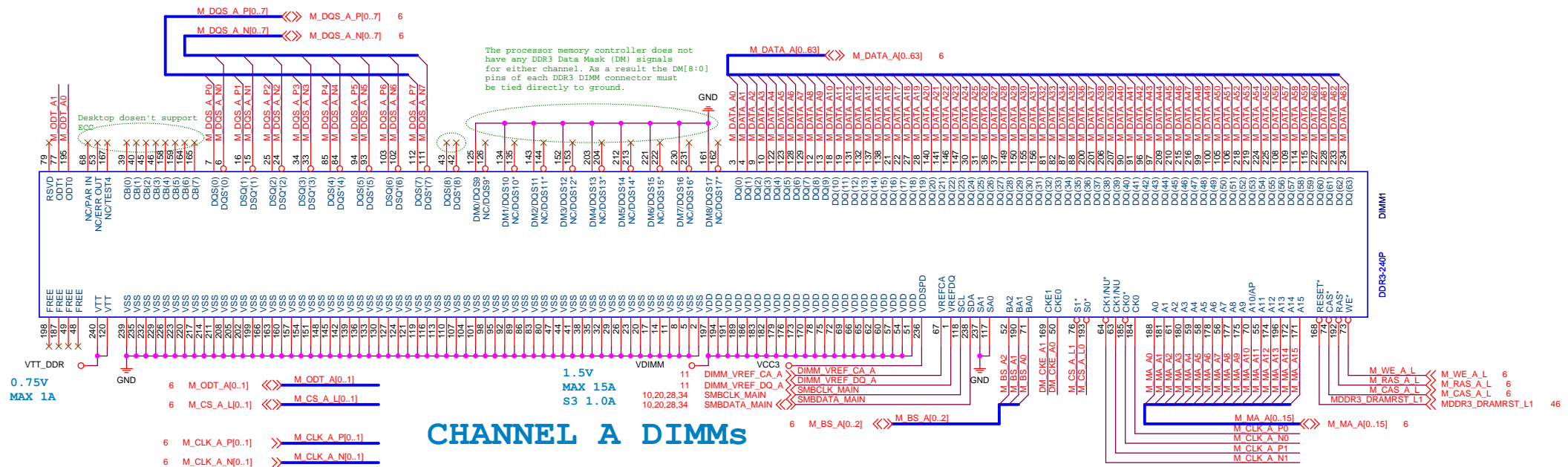
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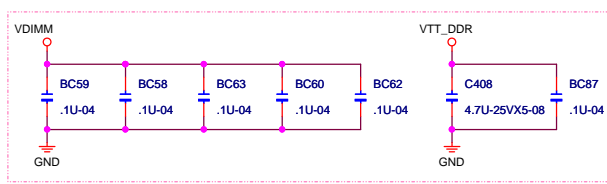
CPU1I				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM36	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM30	AV3	VSS_184	VSS_274	H2
A35	VSS_005	VSS_095	AM37	AV7	VSS_185	VSS_275	H23
AA33	VSS_006	VSS_096	AM38	AV38	VSS_186	VSS_276	H26
AA34	VSS_007	VSS_097	AM39	AV6	VSS_187	VSS_277	H29
AA35	VSS_008	VSS_098	AM40	AW10	VSS_188	VSS_278	H33
AA36	VSS_009	VSS_099	AM44	AW11	VSS_189	VSS_279	H39
AA37	VSS_010	VSS_100	AM5	AW14	VSS_190	VSS_280	H35
AA38	VSS_011	VSS_101	AN10	AW16	VSS_191	VSS_281	H37
AA6	VSS_012	VSS_102	AN11	AW36	VSS_192	VSS_282	H5
AB5	VSS_013	VSS_103	AN14	AW6	VSS_193	VSS_283	H6
AC1	VSS_014	VSS_104	AN17	AY11	VSS_194	VSS_284	H17
AC6	VSS_015	VSS_105	AN19	AY14	VSS_195	VSS_285	H9
AD33	VSS_016	VSS_106	AN22	AY18	VSS_196	VSS_286	J11
AD36	VSS_017	VSS_107	AN24	AY5	VSS_197	VSS_287	J20
AD38	VSS_018	VSS_108	AN27	AY6	VSS_198	VSS_288	J23
AD39	VSS_019	VSS_109	AN30	AY4	VSS_199	VSS_289	J26
AD40	VSS_020	VSS_110	AN31	AY8	VSS_200	VSS_290	J29
AD5	VSS_021	VSS_111	AN32	B10	VSS_201	VSS_291	J32
AD6	VSS_022	VSS_112	AN33	B13	VSS_202	VSS_292	K1
AE3	VSS_023	VSS_113	AN34	B14	VSS_203	VSS_293	K12
AE33	VSS_024	VSS_114	AN35	B17	VSS_204	VSS_294	K13
AE36	VSS_025	VSS_115	AN36	B23	VSS_205	VSS_295	K14
AF1	VSS_026	VSS_116	AN6	B26	VSS_206	VSS_296	K17
AF36	VSS_027	VSS_117	AN6	B29	VSS_207	VSS_297	K2
AF37	VSS_028	VSS_118	AN7	B32	VSS_208	VSS_298	K20
AF40	VSS_029	VSS_119	AN8	B35	VSS_209	VSS_299	K23
AF5	VSS_030	VSS_120	AN9	B38	VSS_210	VSS_300	K26
AF5	VSS_031	VSS_121	AP1	B6	VSS_211	VSS_301	K29
AF6	VSS_032	VSS_122	AP11	C11	VSS_212	VSS_302	K33
AF7	VSS_033	VSS_123	AP14	C12	VSS_213	VSS_303	K35
AG36	VSS_034	VSS_124	AP17	C17	VSS_214	VSS_304	K37
AH2	VSS_035	VSS_125	AP22	C20	VSS_215	VSS_305	K39
AH3	VSS_036	VSS_126	AP25	C23	VSS_216	VSS_306	K5
AH33	VSS_037	VSS_127	AP27	C26	VSS_217	VSS_307	L10
AH36	VSS_038	VSS_128	AP30	C29	VSS_218	VSS_308	L17
AH37	VSS_039	VSS_129	AP36	C32	VSS_219	VSS_309	L20
AH38	VSS_040	VSS_130	AP37	C35	VSS_220	VSS_310	L23
AH39	VSS_041	VSS_131	AP40	C7	VSS_221	VSS_311	L26
AH40	VSS_042	VSS_132	AP44	C8	VSS_222	VSS_312	L29
AH5	VSS_043	VSS_133	AP5	D17	VSS_223	VSS_313	L8
AH8	VSS_044	VSS_134	AR11	D2	VSS_224	VSS_314	M1
AJ12	VSS_045	VSS_135	AR17	D20	VSS_225	VSS_315	M17
AJ18	VSS_046	VSS_136	AR18	D23	VSS_226	VSS_316	M2
AJ21	VSS_047	VSS_137	AR19	D26	VSS_227	VSS_317	M20
AJ25	VSS_048	VSS_138	AR27	D29	VSS_228	VSS_318	M23
AJ27	VSS_049	VSS_139	AR27	D32	VSS_229	VSS_319	M26
AJ36	VSS_050	VSS_140	AR30	D37	VSS_230	VSS_320	M29
AJ36	VSS_051	VSS_141	AR36	D39	VSS_231	VSS_321	M33
AJ5	VSS_052	VSS_142	AR5	D4	VSS_232	VSS_322	M35
AK1	VSS_053	VSS_143	AT1	D5	VSS_233	VSS_323	M37
AK10	VSS_054	VSS_144	AT10	D9	VSS_234	VSS_324	M39
AK13	VSS_055	VSS_145	AT12	D11	VSS_235	VSS_325	M43
AK14	VSS_056	VSS_146	AT15	E12	VSS_236	VSS_326	M47
AK16	VSS_057	VSS_147	AT16	E17	VSS_237	VSS_327	M5
AK22	VSS_058	VSS_148	AT17	E20	VSS_238	VSS_328	M6
AK28	VSS_059	VSS_149	AT17	E23	VSS_239	VSS_329	M9
AK31	VSS_060	VSS_150	AT20	E26	VSS_240	VSS_330	P1
AK32	VSS_061	VSS_151	AT25	E29	VSS_241	VSS_331	P2
AK33	VSS_062	VSS_152	AT27	E36	VSS_242	VSS_332	P36
AK34	VSS_063	VSS_153	AT29	E7	VSS_243	VSS_333	P38
AK35	VSS_064	VSS_154	AT3	E8	VSS_244	VSS_334	P40
AK36	VSS_065	VSS_155	AT3	E7	VSS_245	VSS_335	P5
AK37	VSS_066	VSS_156	AT30	F1	VSS_246	VSS_336	P6
AK4	VSS_067	VSS_157	AT31	F10	VSS_247	VSS_337	P33
AK40	VSS_068	VSS_158	AT32	F13	VSS_248	VSS_338	R35
AK5	VSS_069	VSS_159	AT33	F14	VSS_249	VSS_339	R37
AK6	VSS_070	VSS_160	AT34	F17	VSS_250	VSS_340	R39
AK7	VSS_071	VSS_161	AT35	F2	VSS_251	VSS_341	R8
AK8	VSS_072	VSS_162	AT36	F20	VSS_252	VSS_342	T1
AK9	VSS_073	VSS_163	AT37	F23	VSS_253	VSS_343	T5
AL11	VSS_074	VSS_164	AT38	F26	VSS_254	VSS_344	T6
AL14	VSS_075	VSS_165	AT39	F29	VSS_255	VSS_345	U1
AL17	VSS_076	VSS_166	AT4	F35	VSS_256	VSS_346	V8
AL19	VSS_077	VSS_167	AT40	F37	VSS_257	VSS_347	V2
AL24	VSS_078	VSS_168	AT5	F39	VSS_258	VSS_348	V33
AL27	VSS_079	VSS_169	AT6	F16	VSS_259	VSS_349	V34
AL30	VSS_080	VSS_170	AT7	F6	VSS_260	VSS_350	V35
AL36	VSS_081	VSS_171	AT8	F9	VSS_261	VSS_351	V36
AL5	VSS_082	VSS_172	AT9	G11	VSS_262	VSS_352	V37
AM1	VSS_083	VSS_173	AU1	G12	VSS_263	VSS_353	V38
AM11	VSS_084	VSS_174	AU15	G17	VSS_264	VSS_354	V39
AM14	VSS_085	VSS_175	AU28	G20	VSS_265	VSS_355	V40
AM17	VSS_086	VSS_176	U34	G23	VSS_266	VSS_356	V5
AM2	VSS_087	VSS_177	U6	G26	VSS_267	VSS_357	W6
AM21	VSS_088	VSS_178	AU8	G29	VSS_268	VSS_358	Y5
AM23	VSS_089	VSS_179	AU6	G34	VSS_269	VSS_359	Y8
AM25	VSS_090	VSS_180	AV10	G7	VSS_270	VSS_360	
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02			B3	VSS_NCTF_04		
9 OF 10				10 OF 10			

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

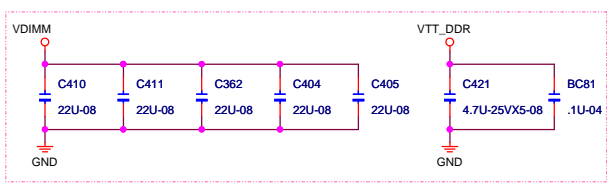


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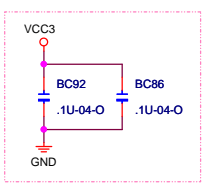
CHA DIMM for WAN



For CHAD1



For CHAD2



PLACE BETWEEN CHA & CHB.
DO NOT PUNCH VIA.

Title
DDR3 - CHA DIMM0/1

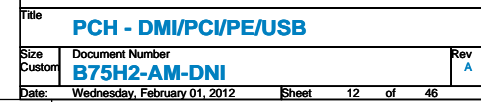
Size
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Document Number
B75H2-AM-DNI

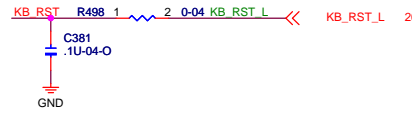
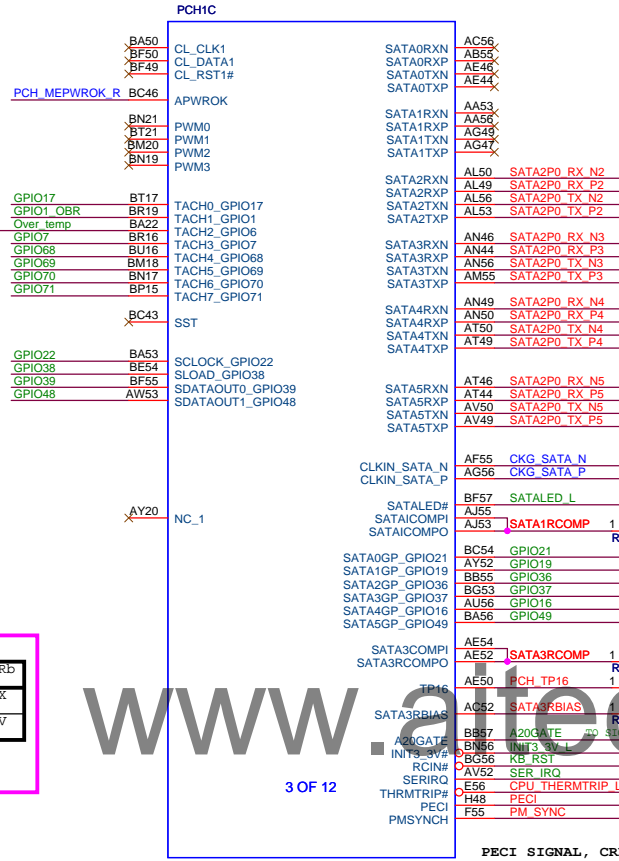
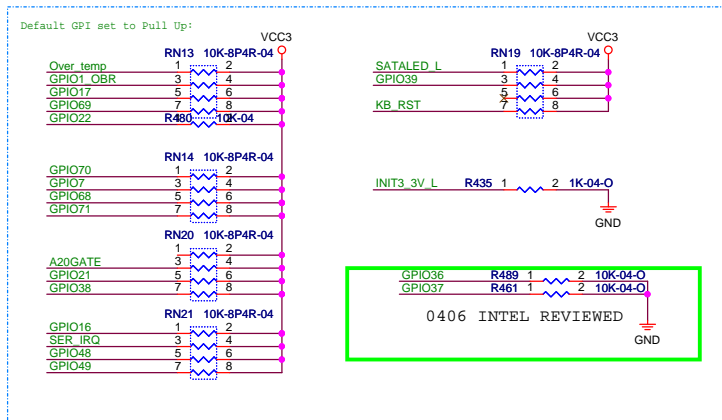
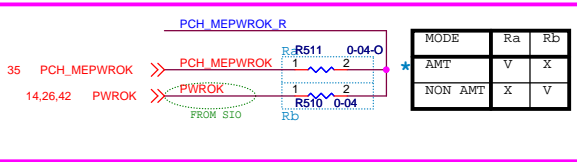
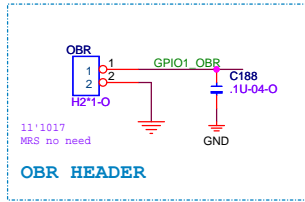
Rev
A

Date: Wednesday, February 01, 2012

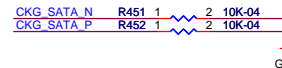
Sheet 9 of 46



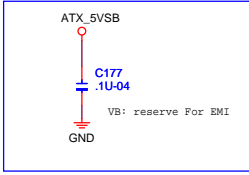
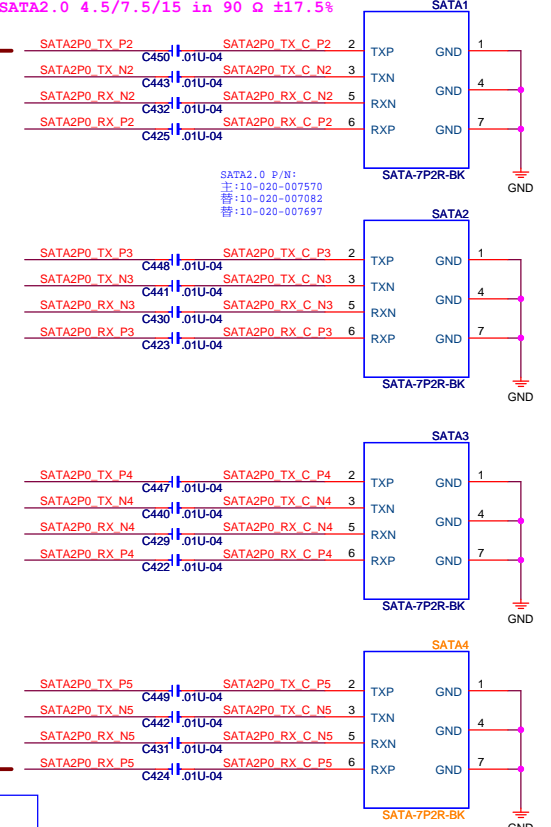
DUAL NET MODE NO NEED SATA3.0

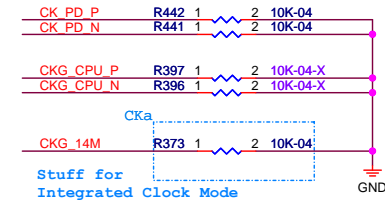
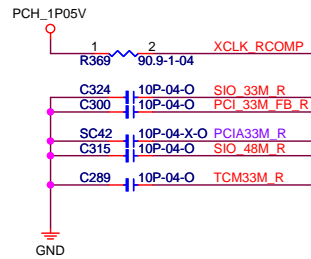


Stuff for Integrated Clock Mode

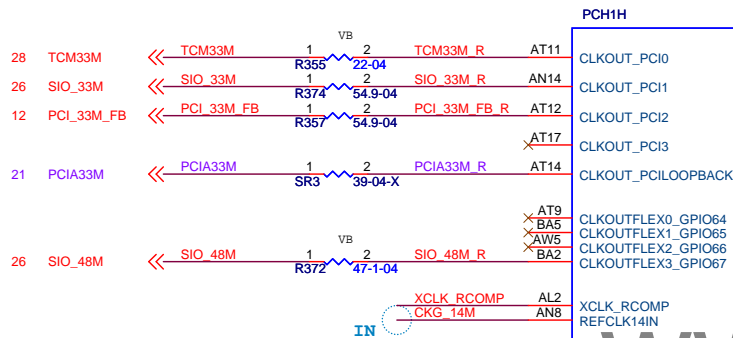


Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

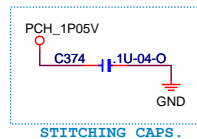
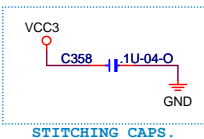
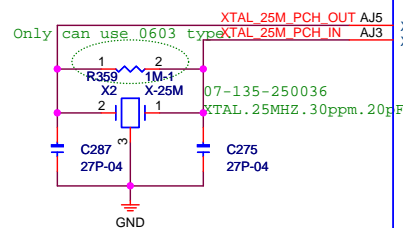




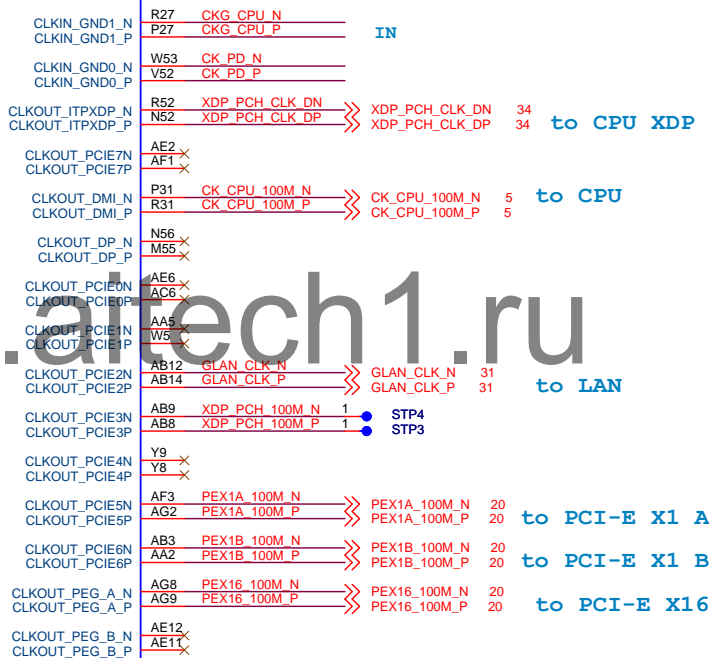
Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X



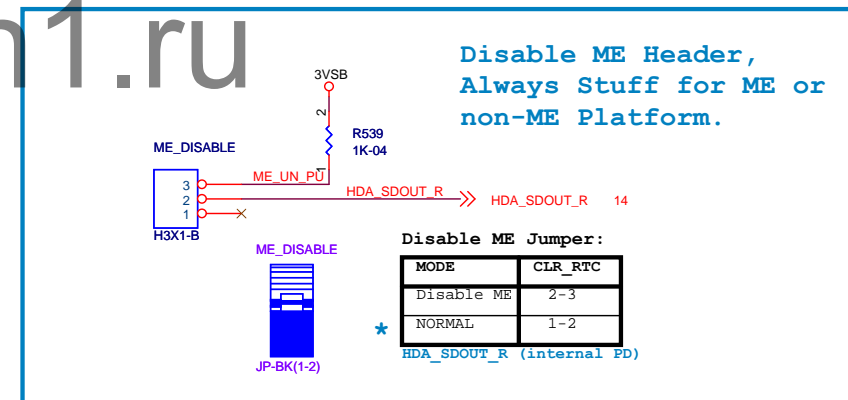
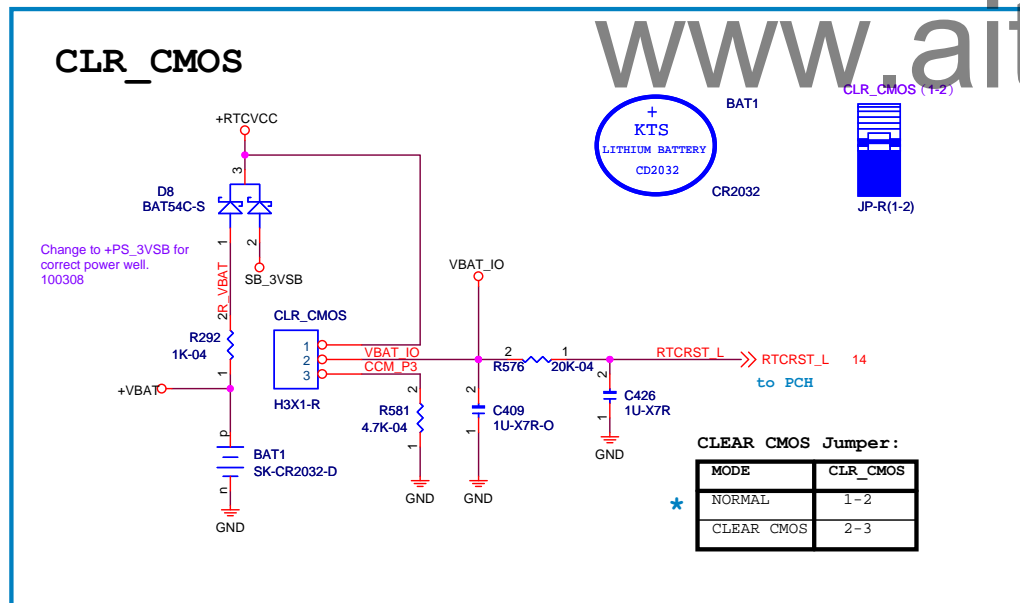
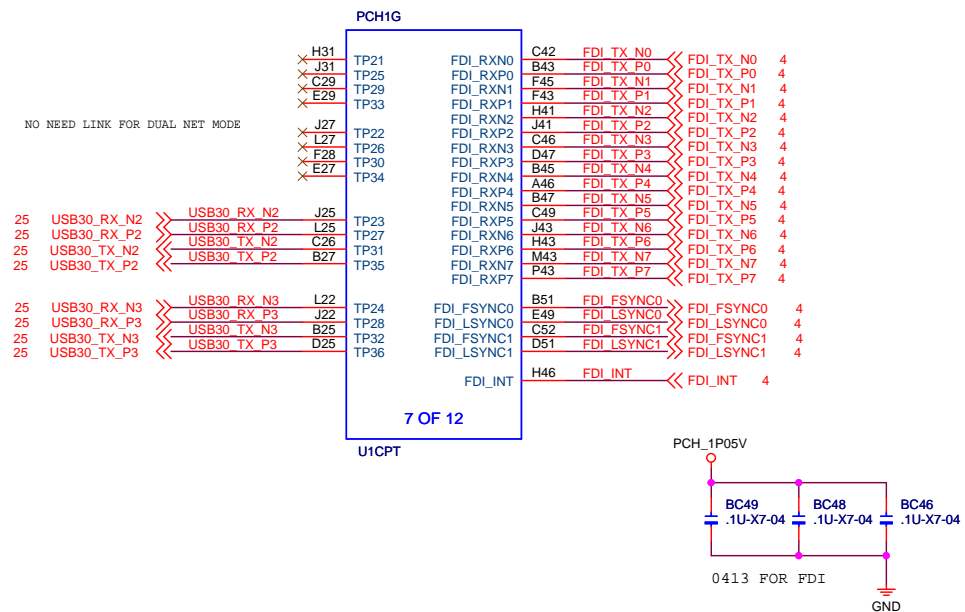
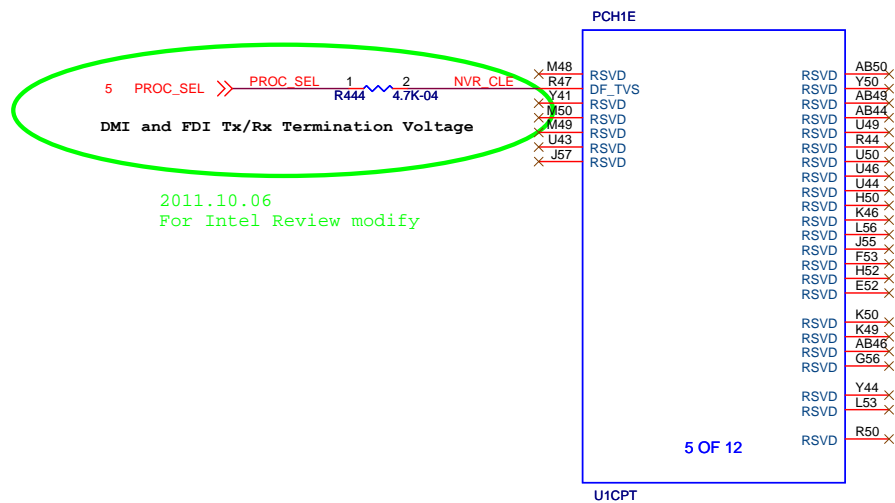
Layout Note:
PCI Clock Max 15000MILS

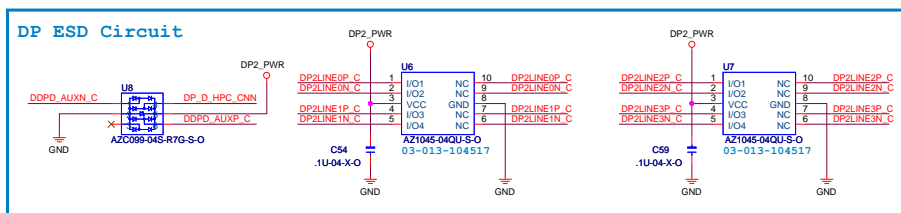
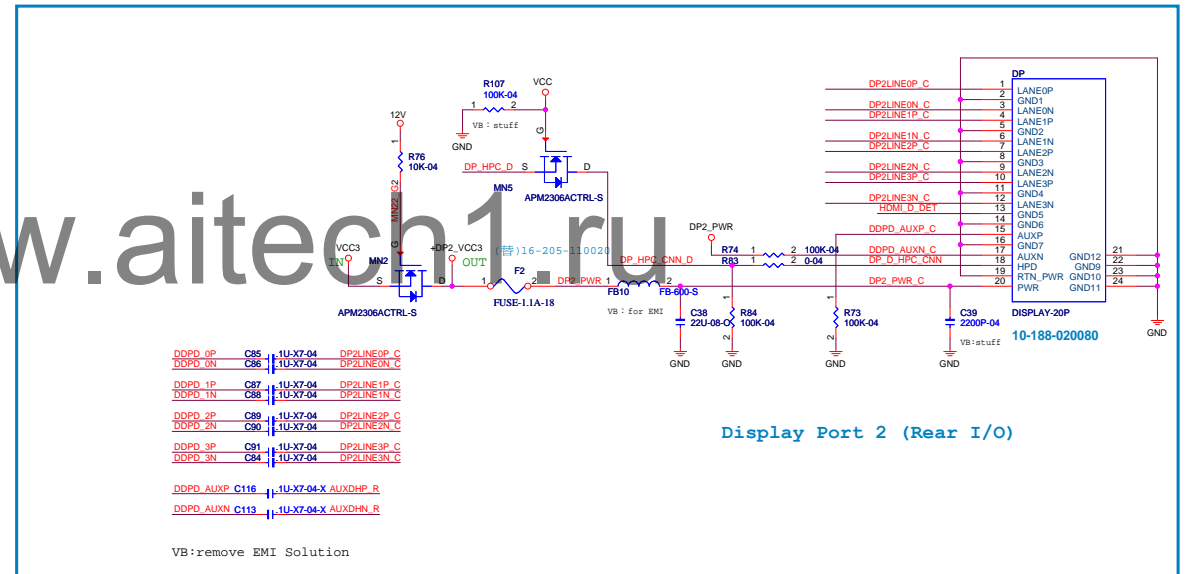
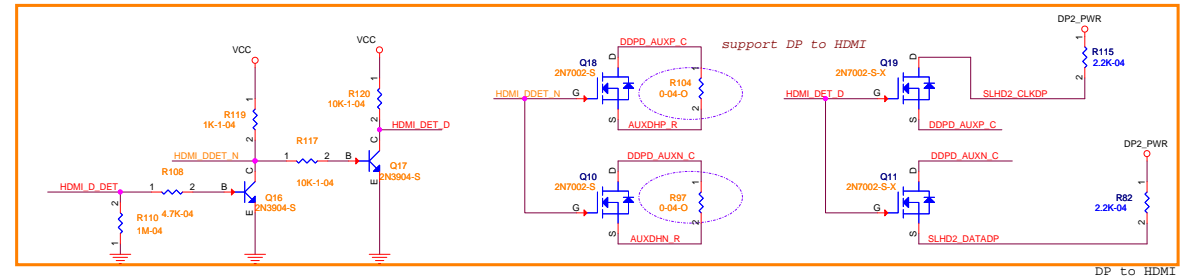
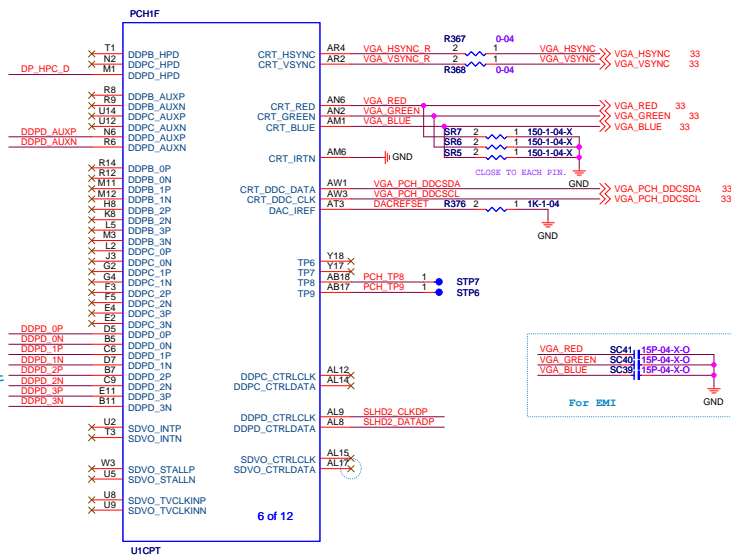


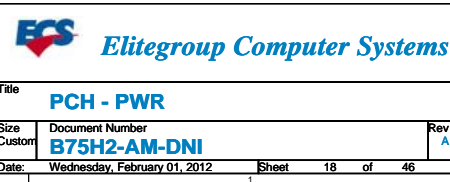
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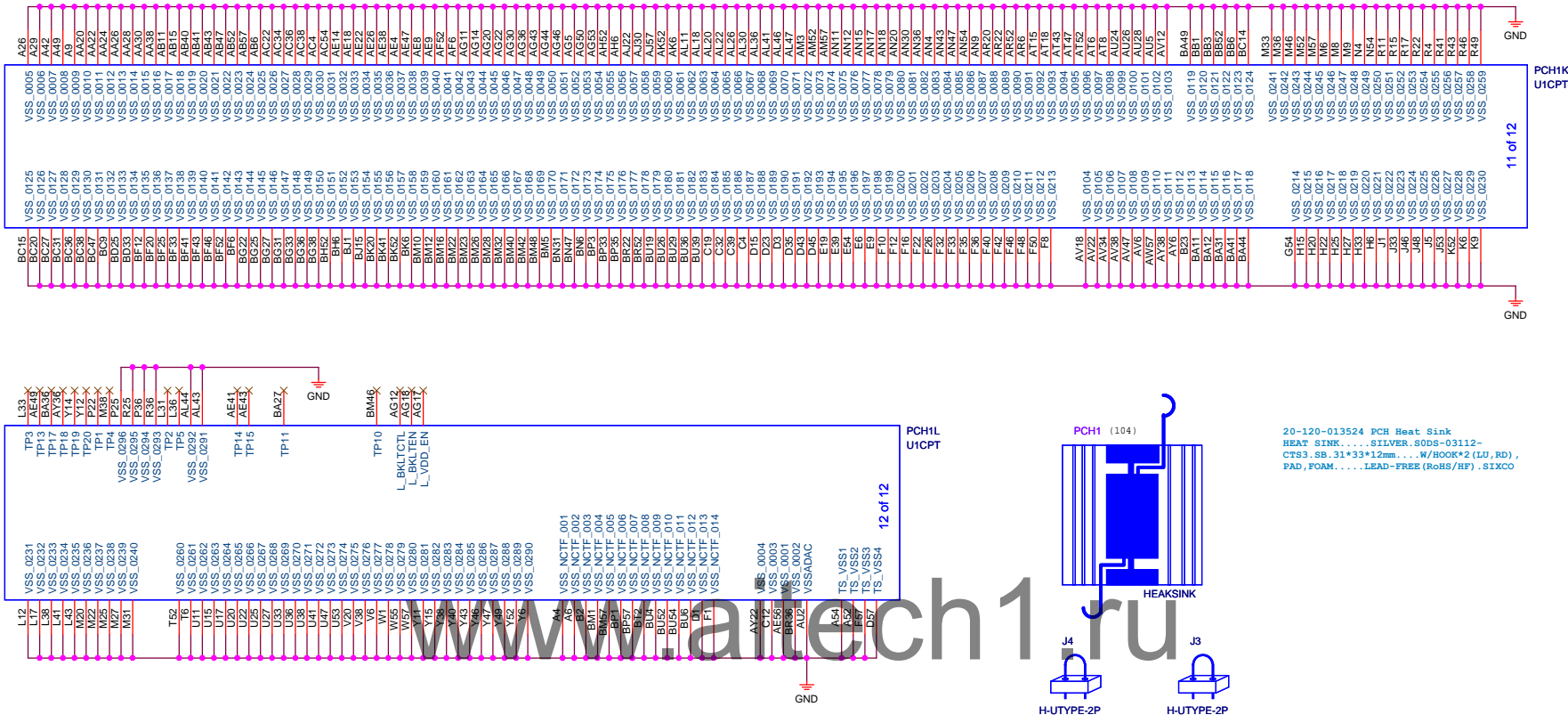


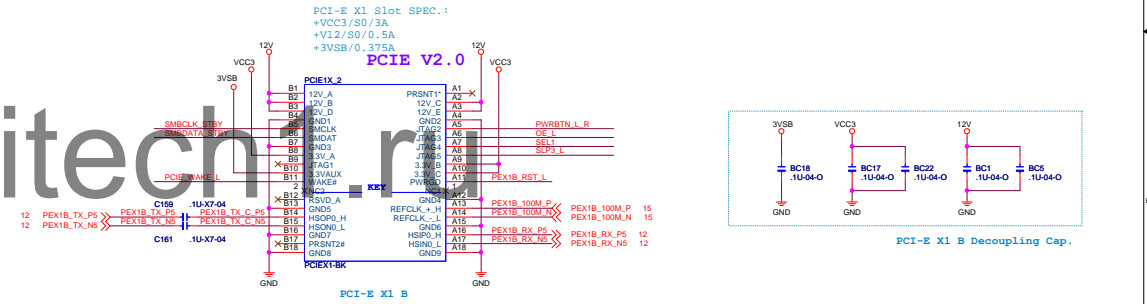
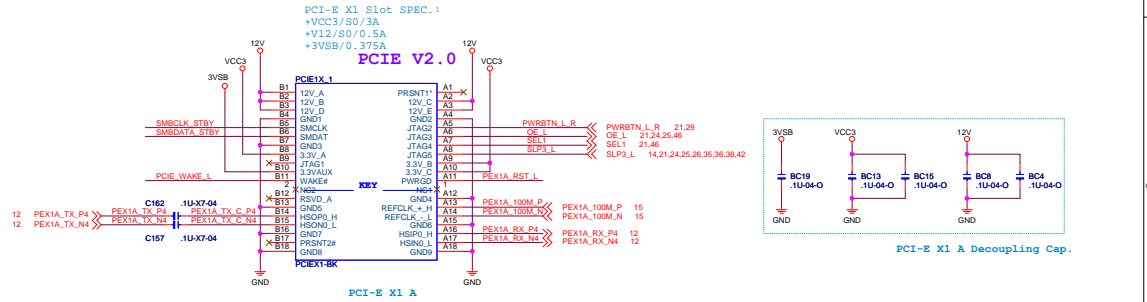
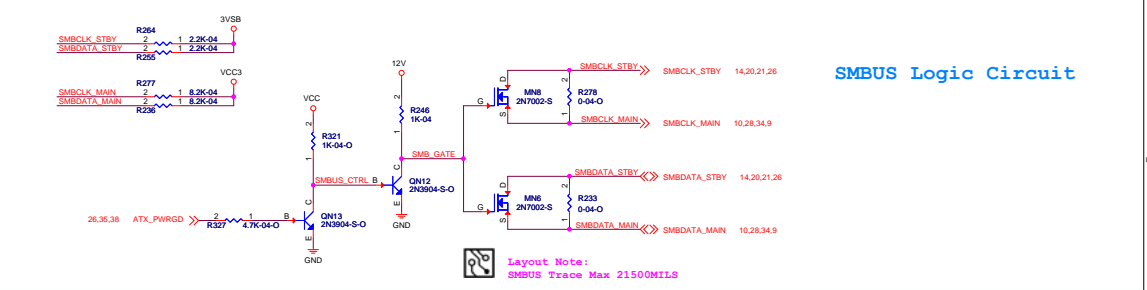
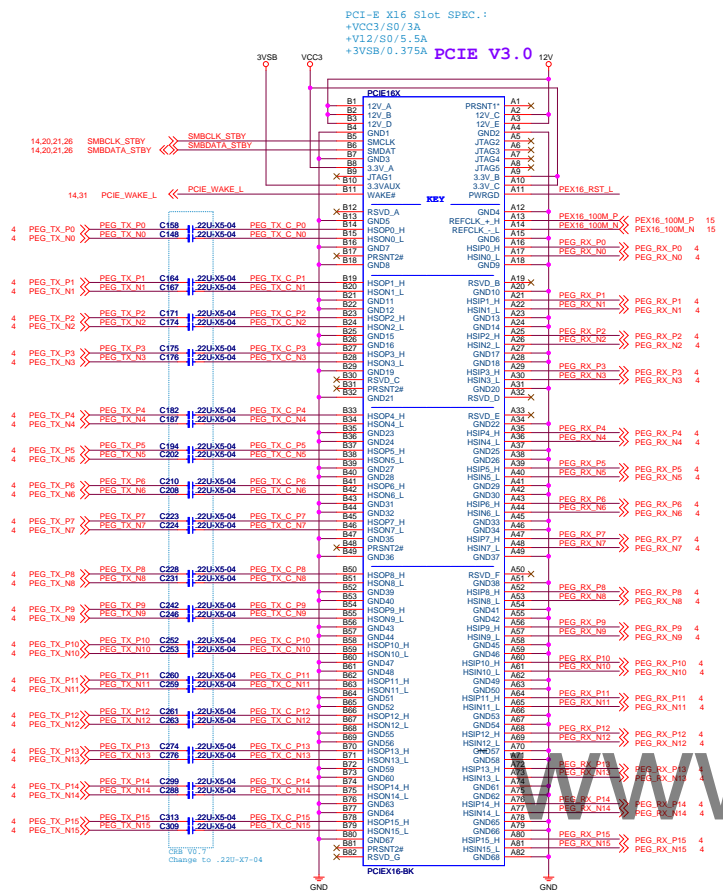
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PCH - CLK IO, CKG - SLG421		
Size	Document Number	Rev
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PWRBTN_L R
OE_L
SEL1
SLP3_L

PWRBTN_L R 20,29
OE_L 20,24,25,46
SEL1 20,46
SLP3_L 14,20,24,25,26,35,36,38,42

PCI V2.3

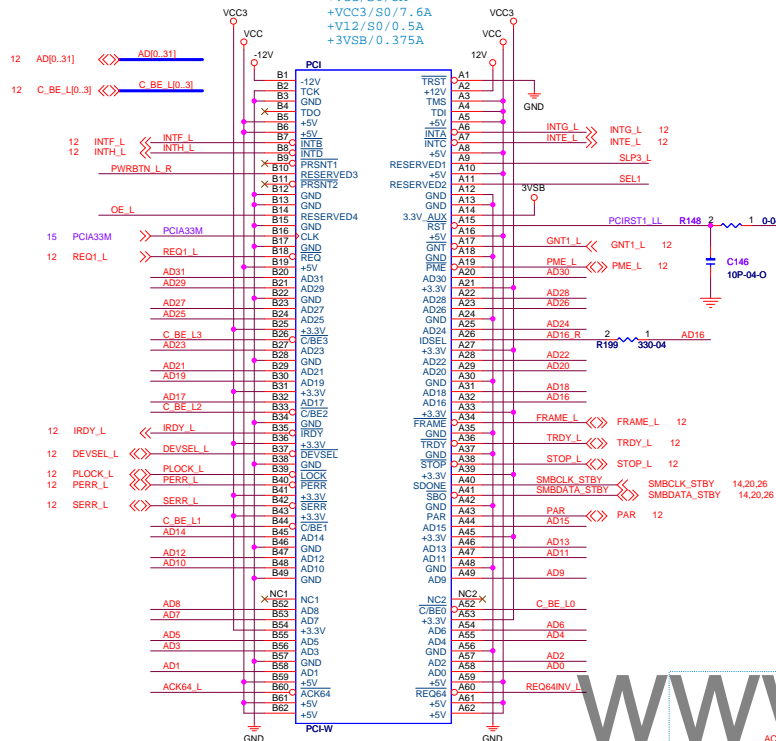
PCI Slot:

+VCC/S0/5A

+VCC3/S0/7.6A

+V12/S0/0.5A

+3VSB/0.375A



INT:G F E H
IDSEL:AD16
REQ/QNT:1

Follow CSB V0.7 Setup

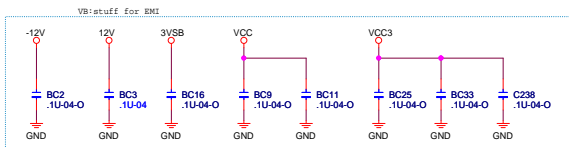
REMOVE PCI SOLT2

SEL1 from PCI/PCIE slot SEL#

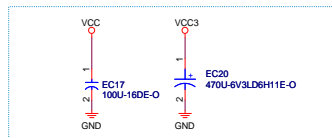
DUAL-NET MODE CONTROL SIGNAL

PCI SLOT	PCIE1 SLOT	CONTROL SIGNAL
A9	A8	SLP_S3#
A11	A7	SEL#
B10	A5	PWRBTN#
B14	A6	OE#

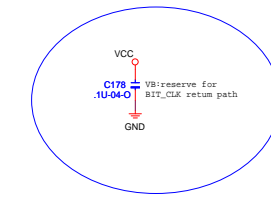
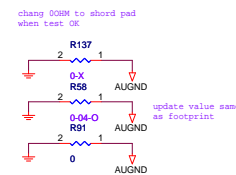
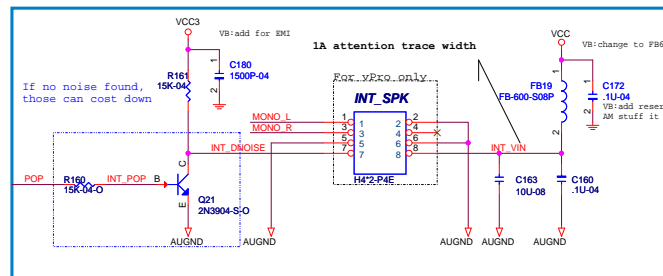
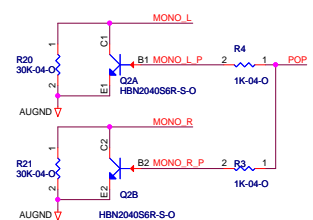
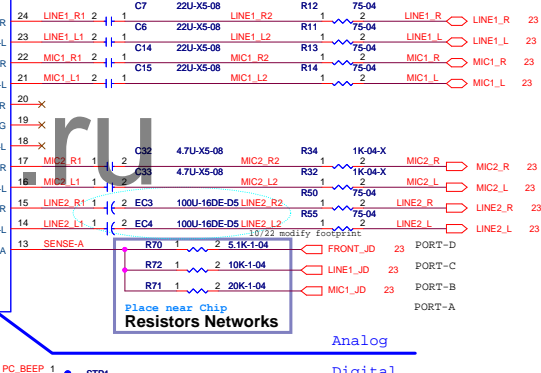
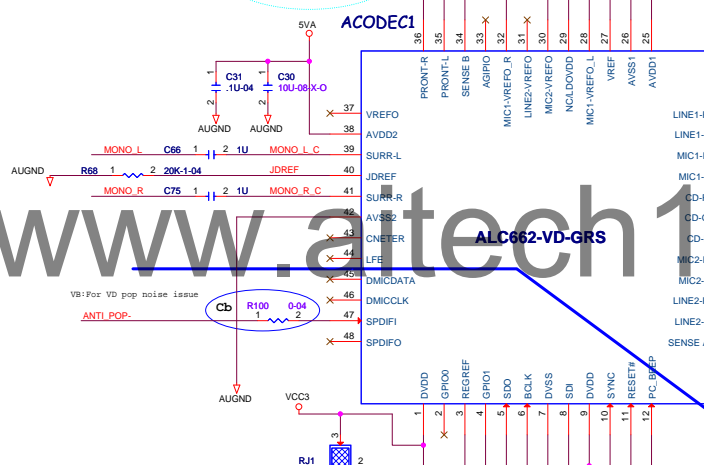
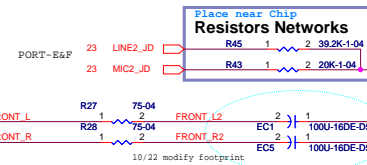
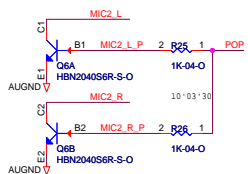
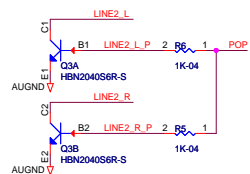
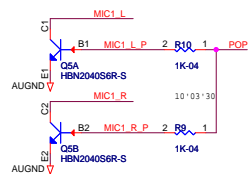
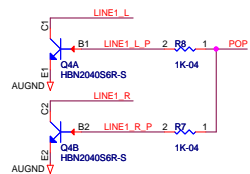
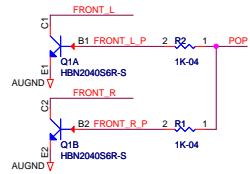
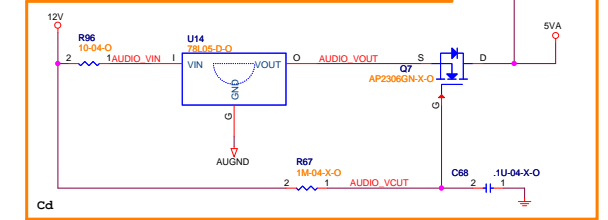
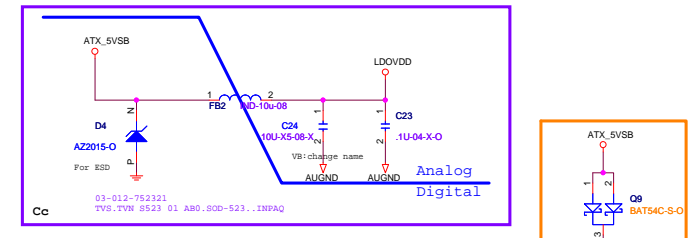
www.aitech1.ru



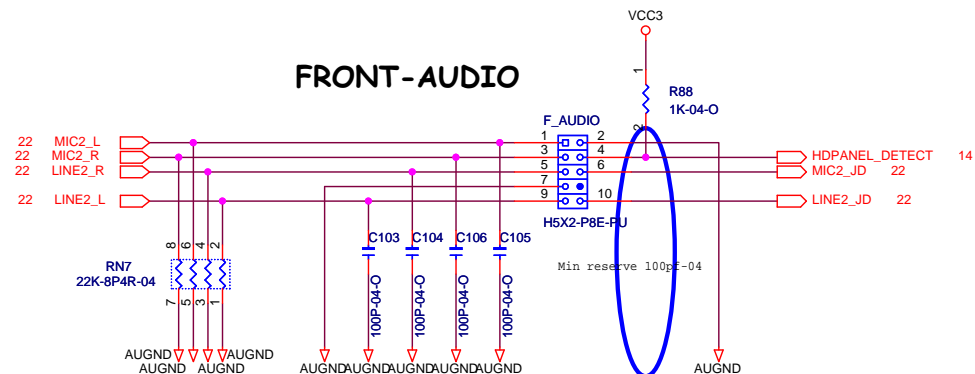
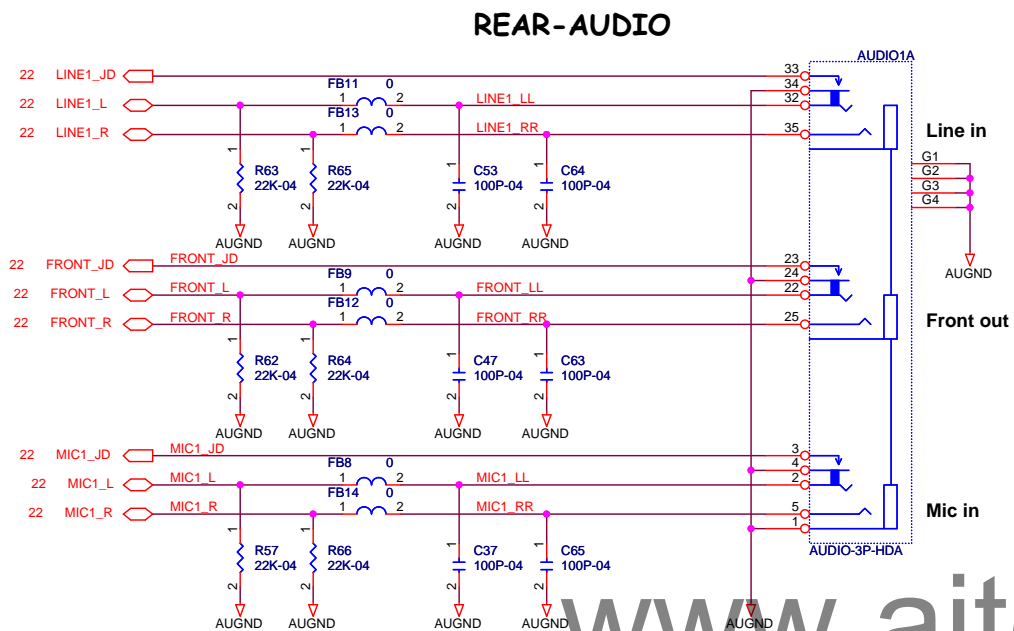
PCI1 Decoupling Cap.



PCI1&PEX1B Decoupling Cap.

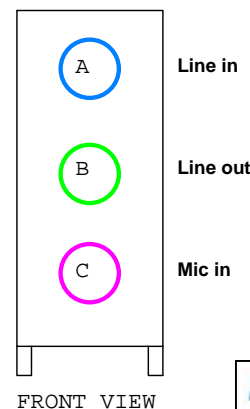
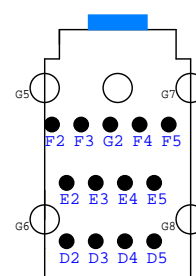
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	ALC662 VC	ALC662 VD
Ca	V	X
Cb	X	V
Cc	X	V
Cd	V	X



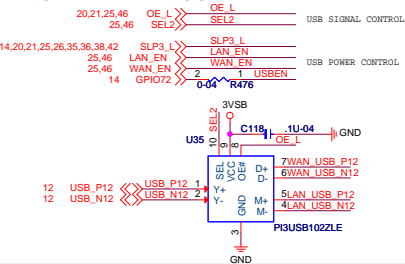
VB:remove SPDIF Circuit

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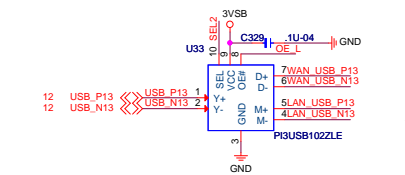


ECS <i>Elitegroup Computer Systems</i>			
AUDIO ALC662 (PANEL)			
Title	AUDIO ALC662 (PANEL)		
Size	Document Number	Rev	
B	B75H2-AM-DNI	A	
Date:	Wednesday, February 01, 2012	Sheet	23 of 46

FRONT PANEL USB HEADER

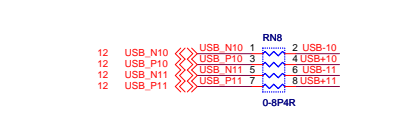


HDR 1

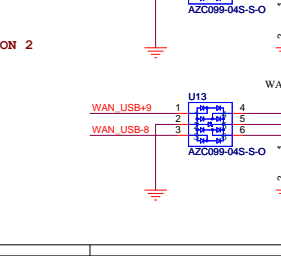
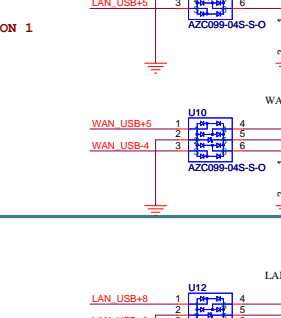
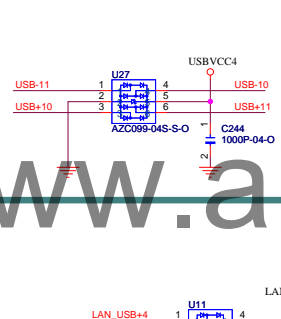
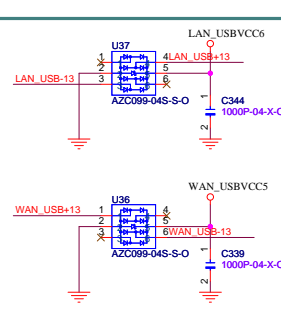
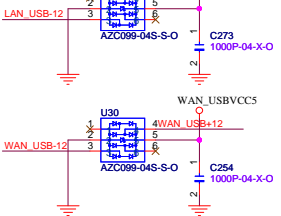
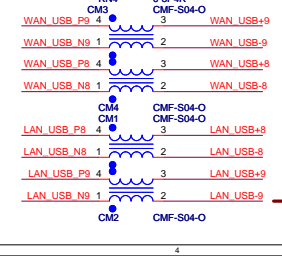
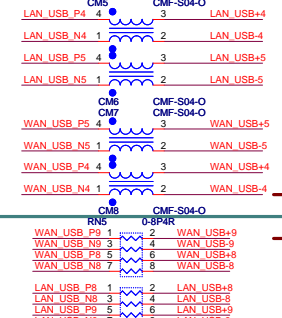
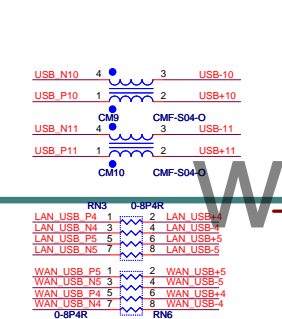
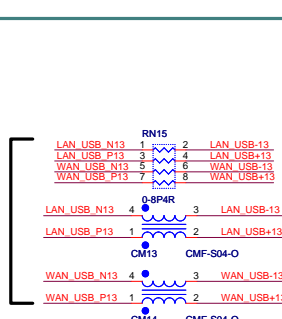
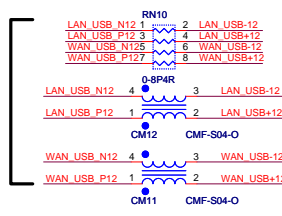
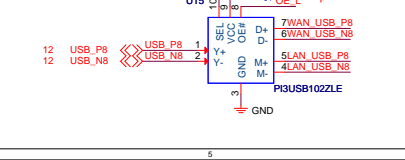
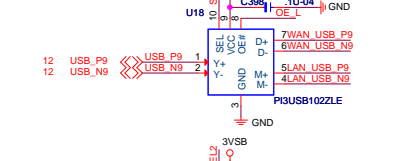
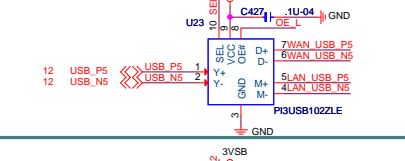
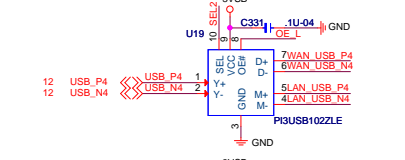


HDR 2

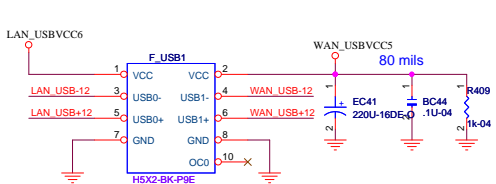
HDR3 FOR DUAL NET MODE CARD



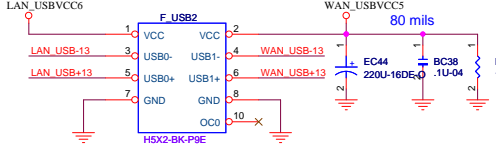
REAR PANEL USB CONNECTOR



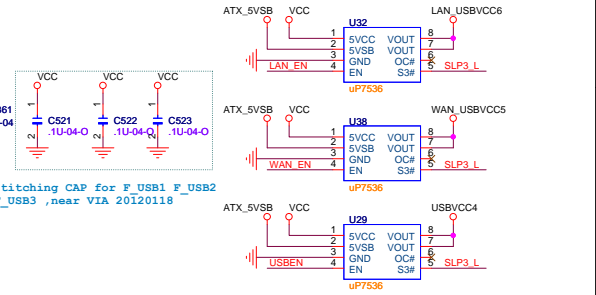
FRONT PANEL USB HEADER 1



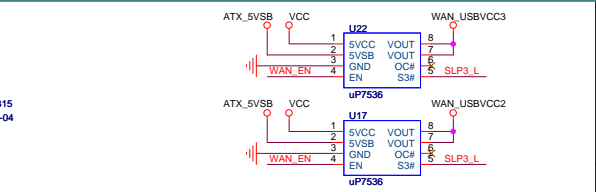
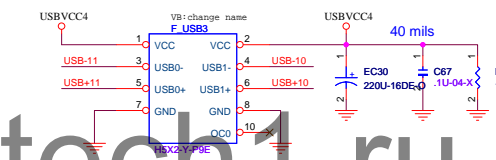
FRONT PANEL USB HEADER 2



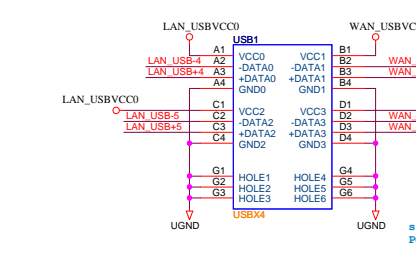
DNI Mode	ACPI State	S0/S3	S4	S5
OE_L=0 enter DNI mode	SLP_S4# Enable state SEL1 =H SEL2=L USB power state USB signal state	SLP_S4# = H LAN_EN WAN_EN Only one system USB power will be hold LAN link WAN link	SLP_S4# = L LAN_EN WAN_EN Two systems USB power will be shut off NA NA	SLP_S4# = L LAN_EN WAN_EN Two systems USB power will be shut off NA NA
OE_L=1 disable DNI mode	OE_L=1	WAN/LAN USB is disable		



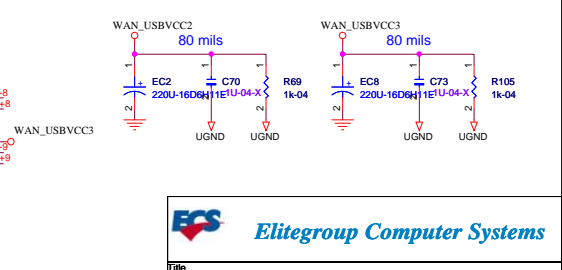
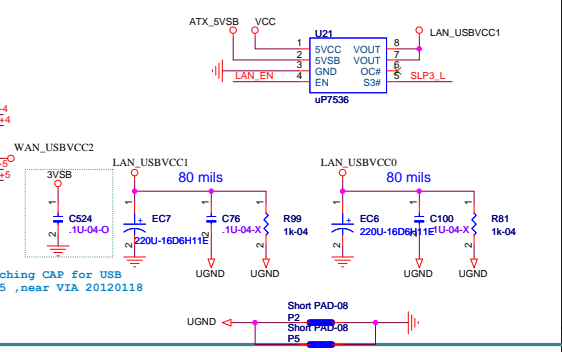
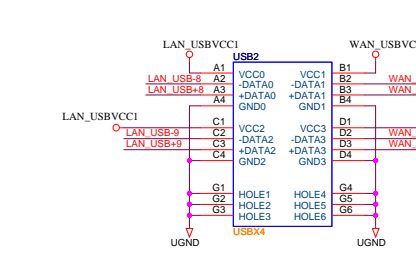
2ports for DUAL MODE Card



REAR PANEL USB2.0 CONNECTOR 1

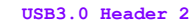
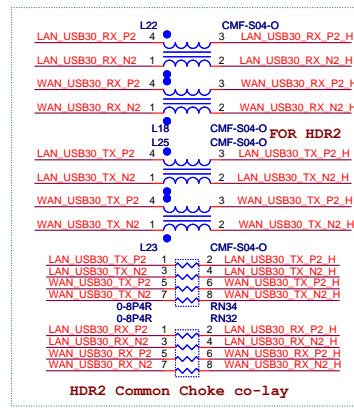
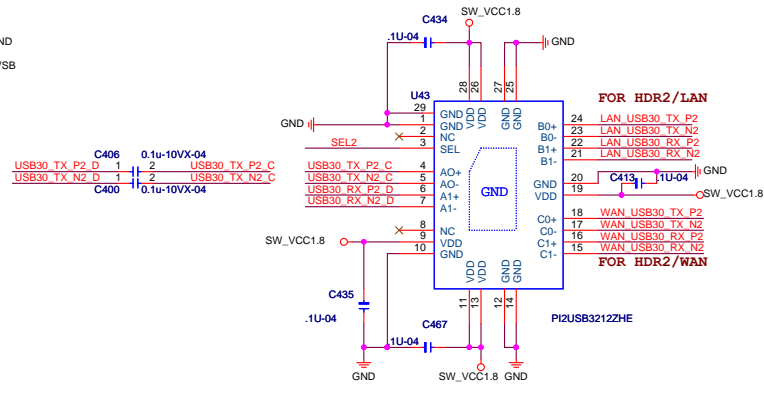


REAR PANEL USB2.0 CONNECTOR 2

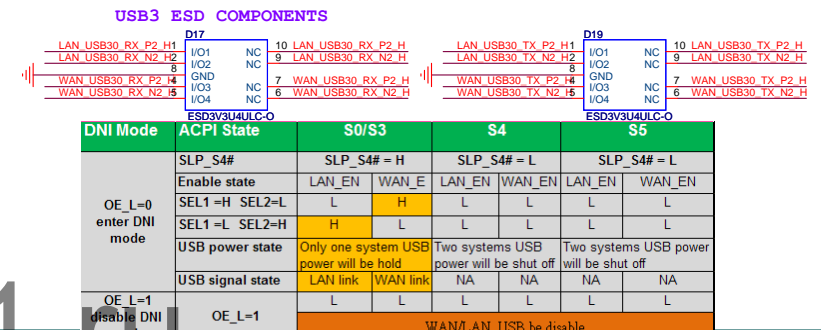
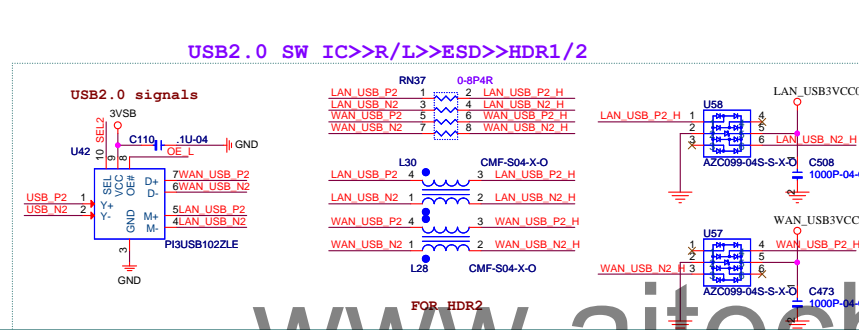


Elitegroup Computer Systems		
DUAL NET MODE USB2.0 SW		
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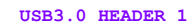
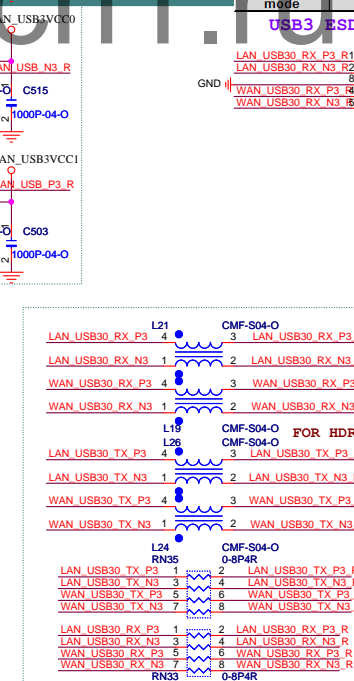
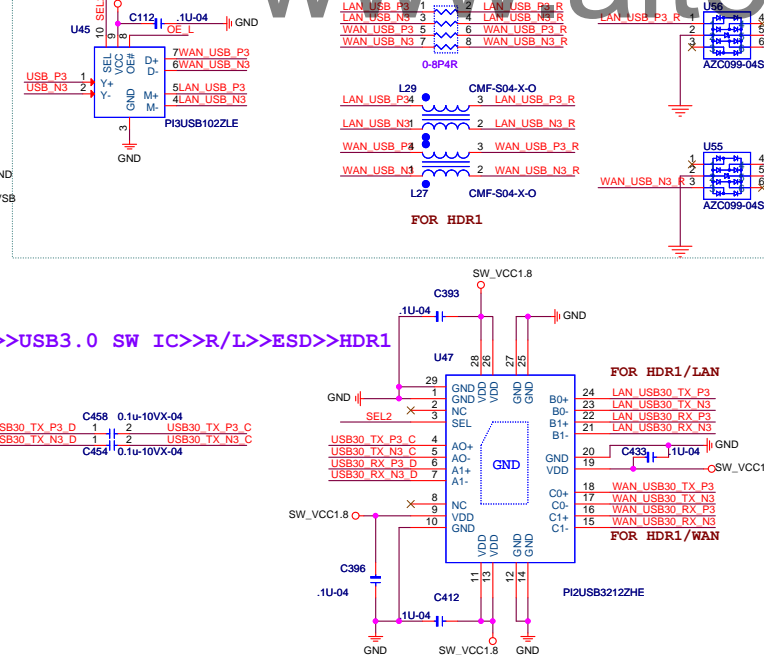
RE-DRIVER>>USB3.0 SW IC>>R/L>>ESD>>HDR2



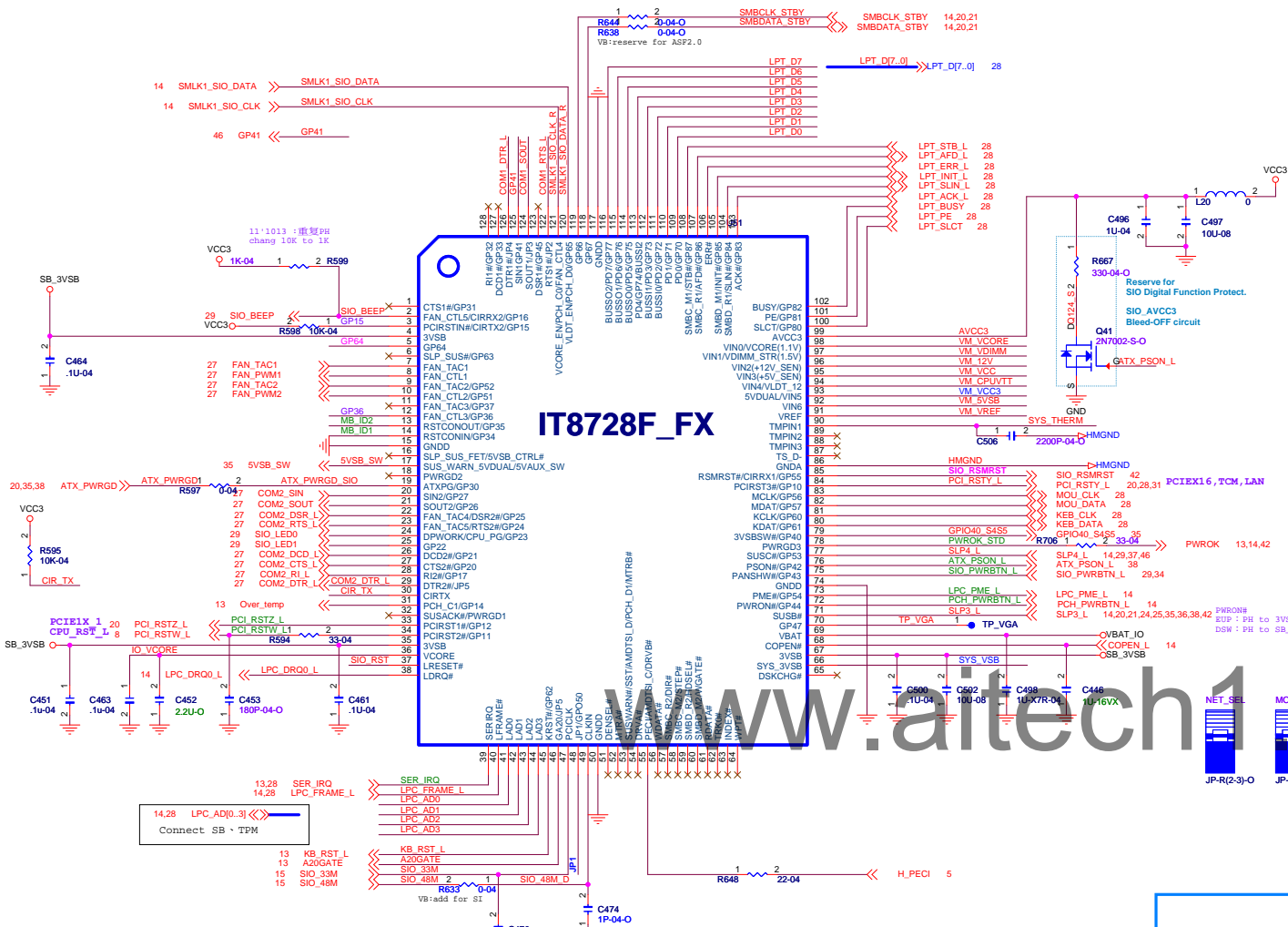
USB3.0 HEADER



The schematic diagram illustrates the USB and LAN interface for the HDRI module. The USB section features a USB P3 connector (pins 1-4) connected to a USB1022LE chip (U45) via a 10 SEL2 pin header. The LAN section shows LAN USB P3 and WAN USB P3 connectors connected to LAN USB N3 and WAN USB N3 pins, which are then connected to LAN USB P3 and WAN USB P3 pins. The LAN section also includes a 0.8P4R resistor (RN36) and a 1000P-04-0 capacitor (C51).



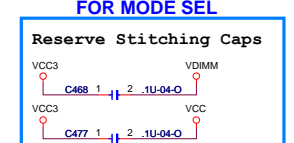
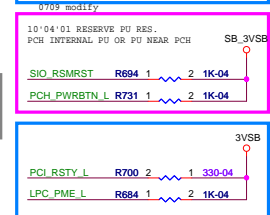
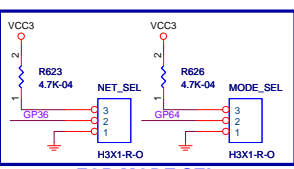
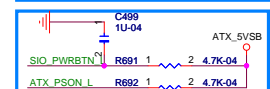
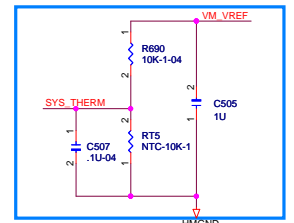
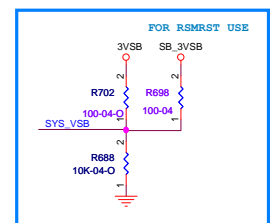
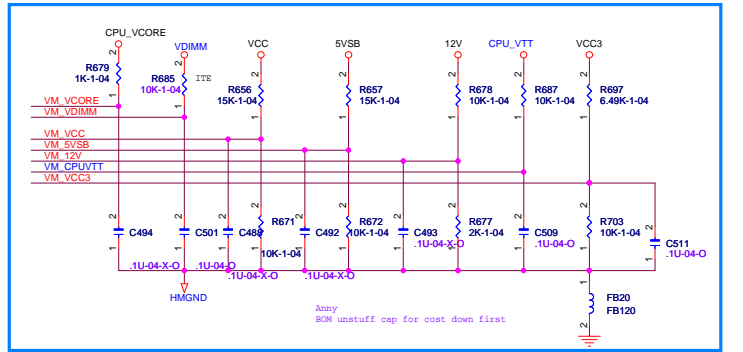
USB3.0 HEADER



IT8728F-FX

TP_VGA	Display Type
LOW	onboard VGA
High	default BIOS

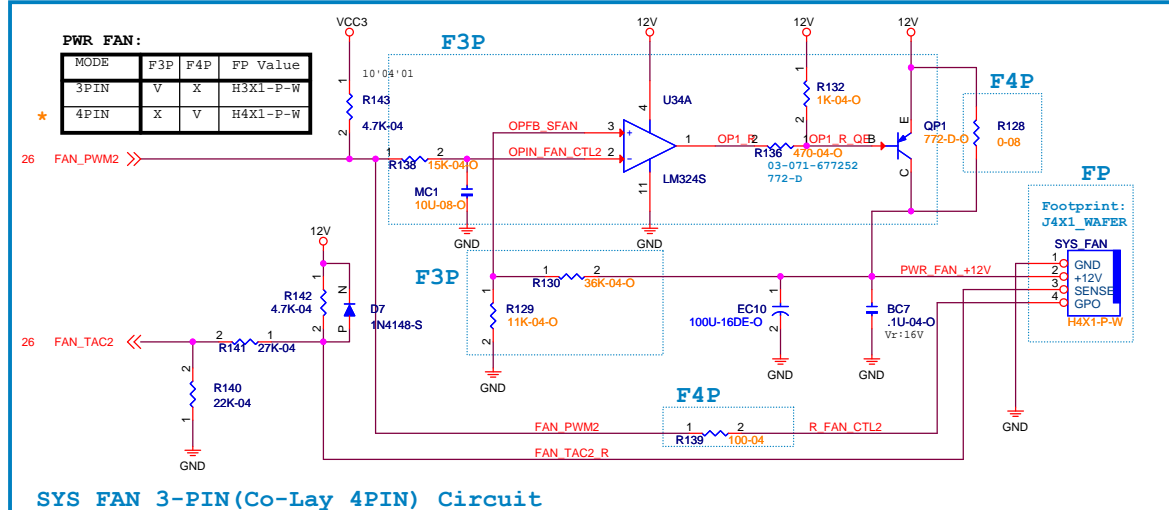
BOARD ID		
VB: Vendor recommend ph for PIN14 effect PWRGD1/2/3 reset		
MB_ID1	MB_ID2	MB_ID3
Default	Hi	Hi
TBD	Hi	Low
TBD	Low	Hi
TBD	Low	Low



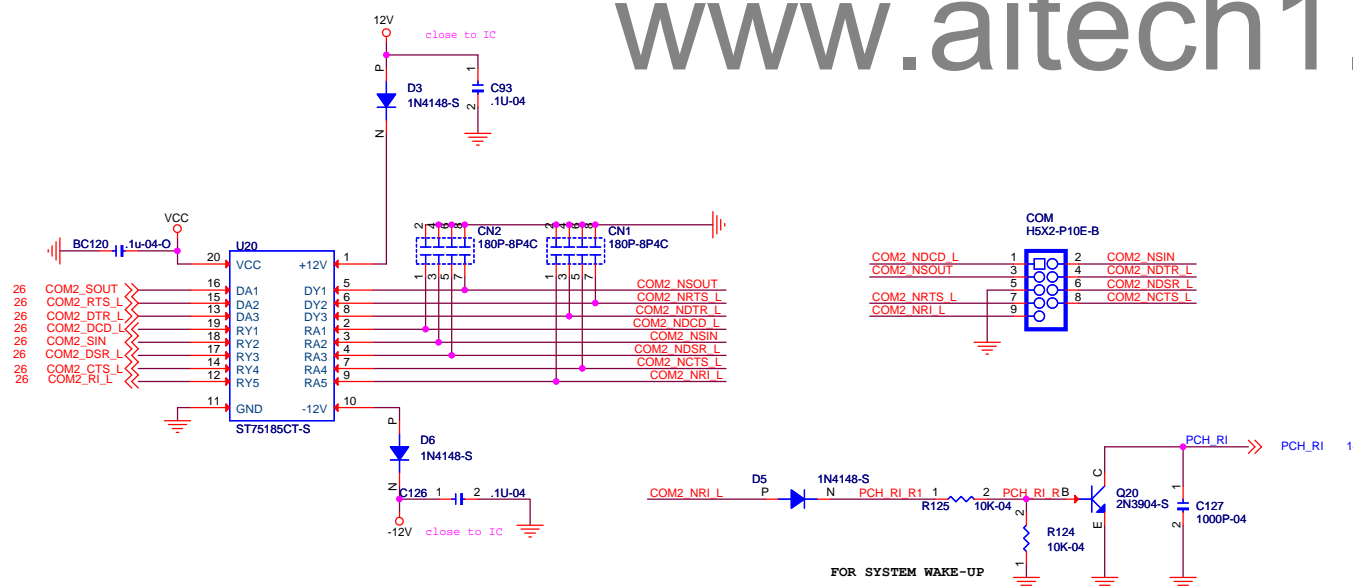
Power-On			
Strapping	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP *
Pin-48	DSW	0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK *
Pin-122		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h *
Pin-124		0	EC Index 63h/6Bh/73h is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence *
Pin-126		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default) *
Pin-29	OV/UV	0	Force Mode

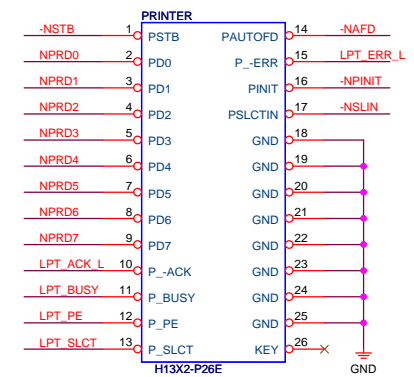
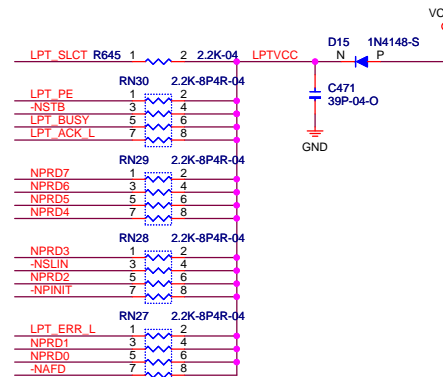
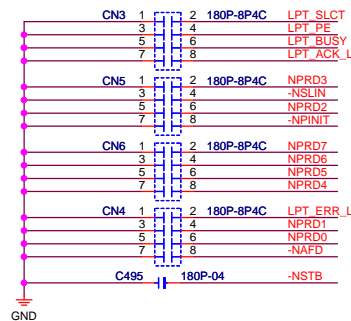
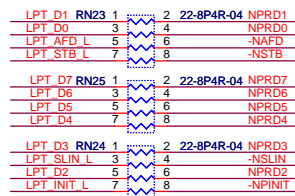
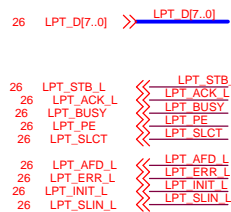


COM PORT I/O



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LPT Header Circuit

TPM CHIP/Header Circuit

14,26 LPC_AD[0..3] >> SB · SIO

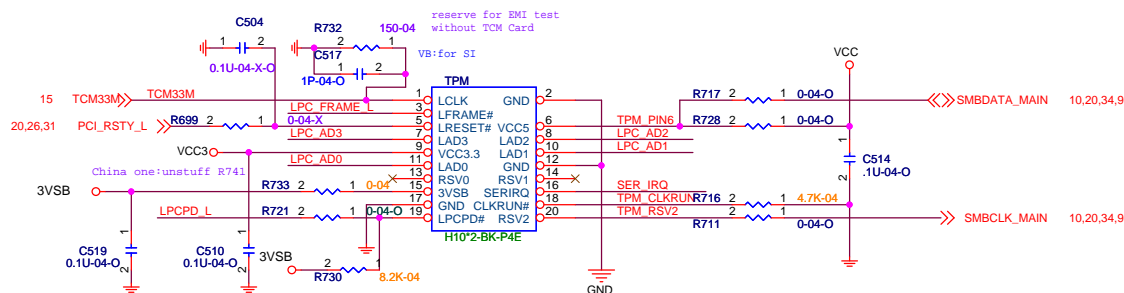
LPCPD_L >> LPCPD_L 14

SER_IRQ >> SER_IRQ 13,26

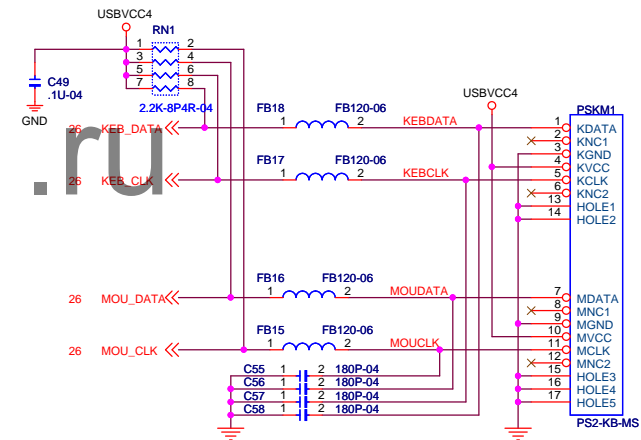
LPC_FRAME_L >> LPC_FRAME_L 14,26

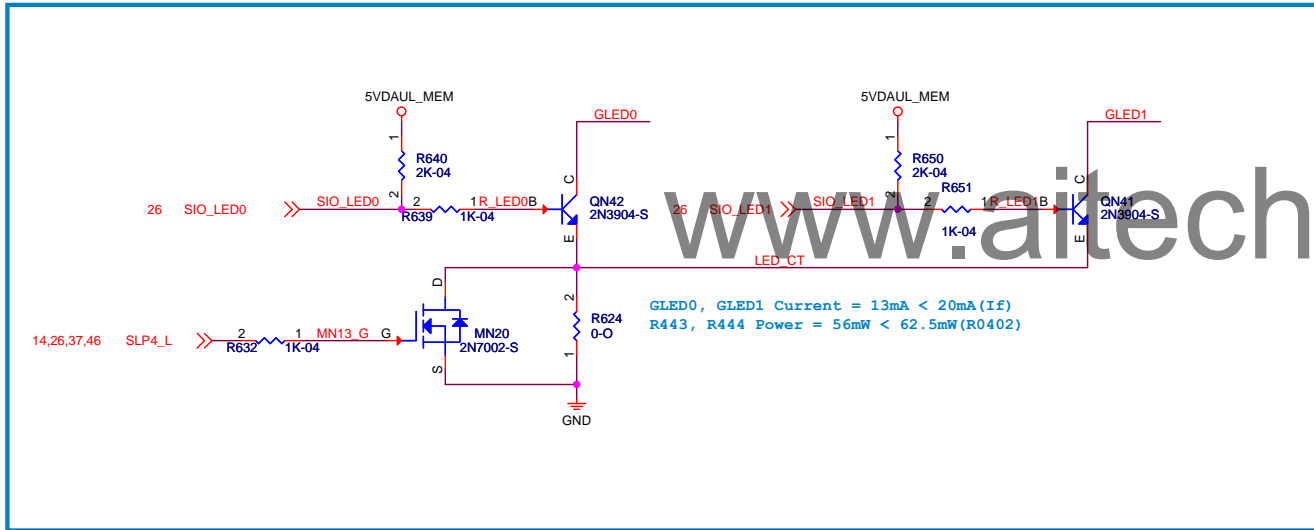
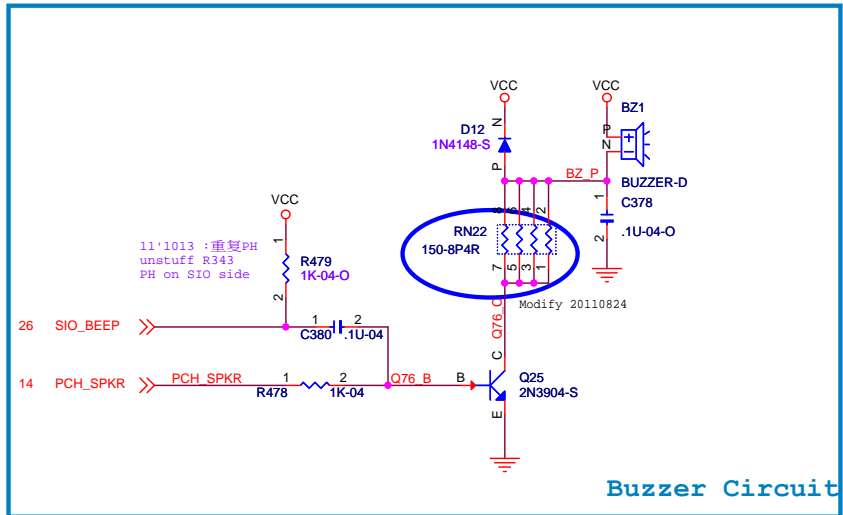
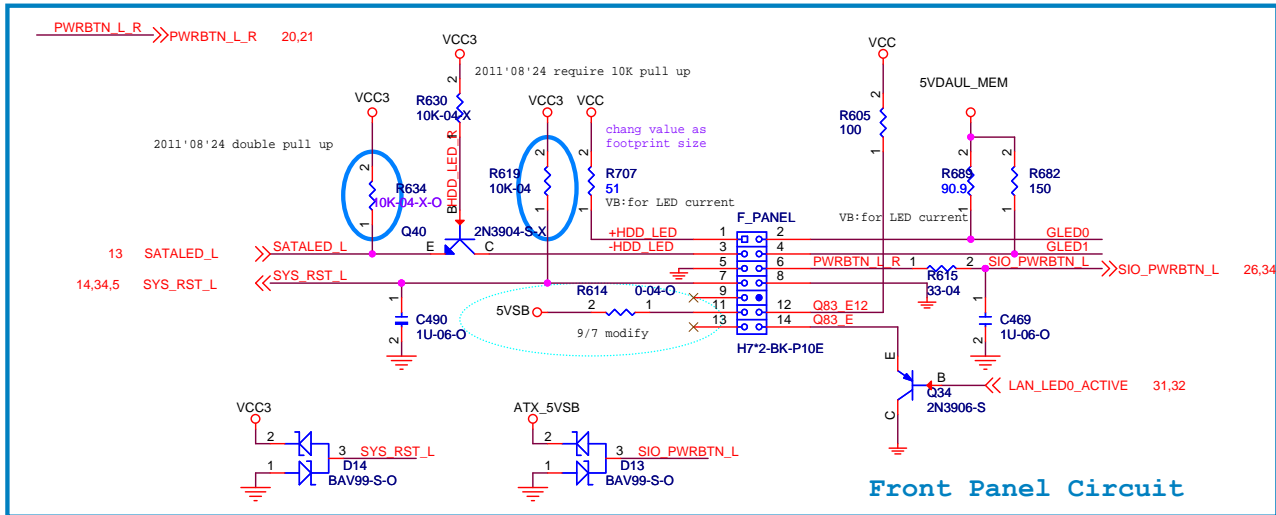
11'1017 Anny
remove colay TPM Chip circuit

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PS2-KB Circuit




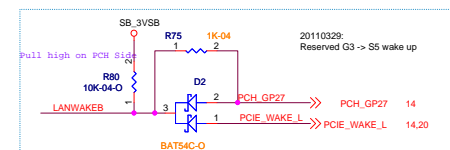
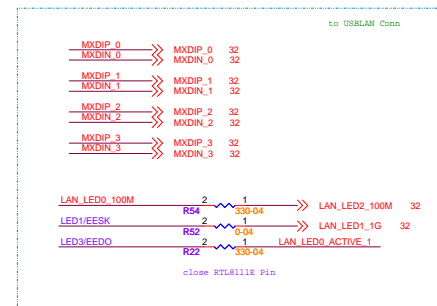
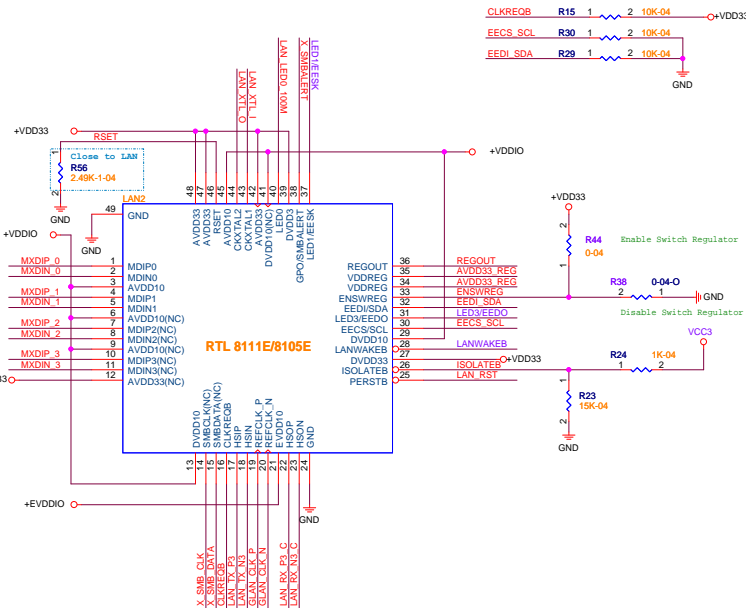
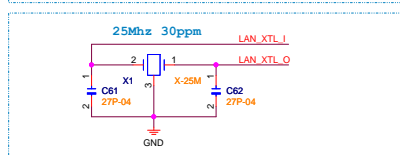
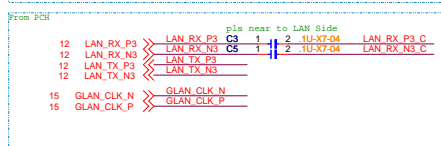
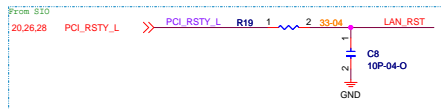


	LED	S0	S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	OFF	OFF

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REMOVE INTEL LAN FOR DUAL NET MODE

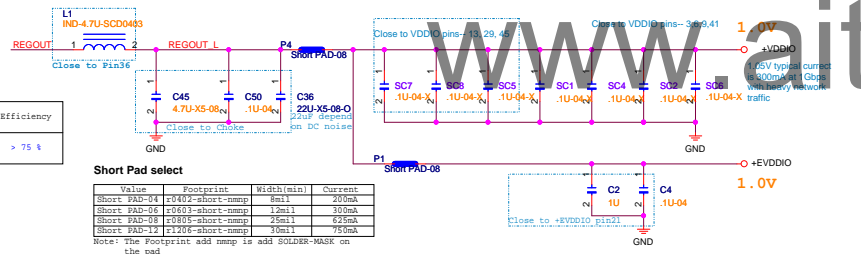
 Elitegroup Computer Systems		
Title TBD		
Size Custom	Document Number B75H2-AM-DNI	Rev A
Date: Wednesday, February 01, 2012	Sheet 30 of 46	1



The power inductor SPEC.

L (uH) / tolerance	ESR (ohm) @ 1MHz	Max IDC (mA)	Efficiency
2.2 or 4.7 / <=20%	< 0.8	> 600	> 75 %

08-403-475170
POWER IND. 4.7uH, 10%, 1.9A, 80m OHM, SMD, 4.5*4*3.2mm, PP104030P-4R7K, LEAD-FREE (RoHS/HP), TAI-TECH



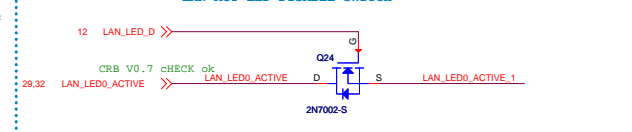
Short Pad select

Value	Footprint	Width (mm)	Current
Short PAD-04	20402-short-nmp	8mil	200mA
Short PAD-06	20603-short-nmp	12mil	300mA
Short PAD-08	20805-short-nmp	25mil	425mA
Short PAD-12	21206-short-nmp	30mil	950mA

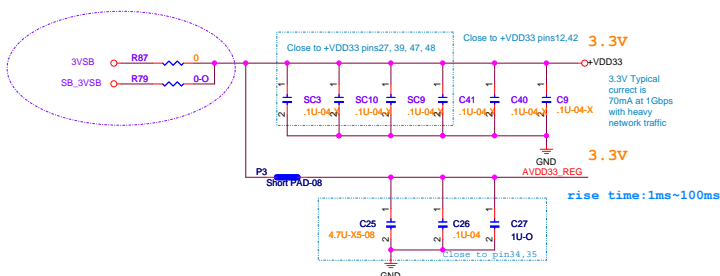
Note: The Footprint add nmp is add SOLDER-MASK on the pad

BOM Different between RTL8111E, RTL8105E:
For RTL8111E Series
*VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.
For RTL8105E-VB
*VDD10 pins-- 3, 13, 29, 45.
For RTL8105E Series (except for VB)
*VDD10 pins-- 13, 29, 45.

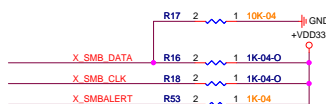
LAN ACT LED DISABLE SWITCH



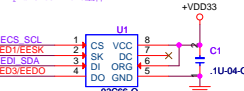
BOM Different between RTL8111E, RTL8105E:
For RTL8111E Series
*VDD33 pins-- 12, 27, 39, 42, 47, 48.
For RTL8105E-VB
*VDD33 pins-- 27, 39, 42, 47, 48.
For RTL8105E Series (except for VB)
*VDD33 pins-- 27, 39, 47, 48.



Acer/FDR request:
1: default use e-FUSE;
2: only reserve External EEPROM;
3: B75 LAN 使用 RTL8111E-VL CG 不用支持 ASF 2.0;



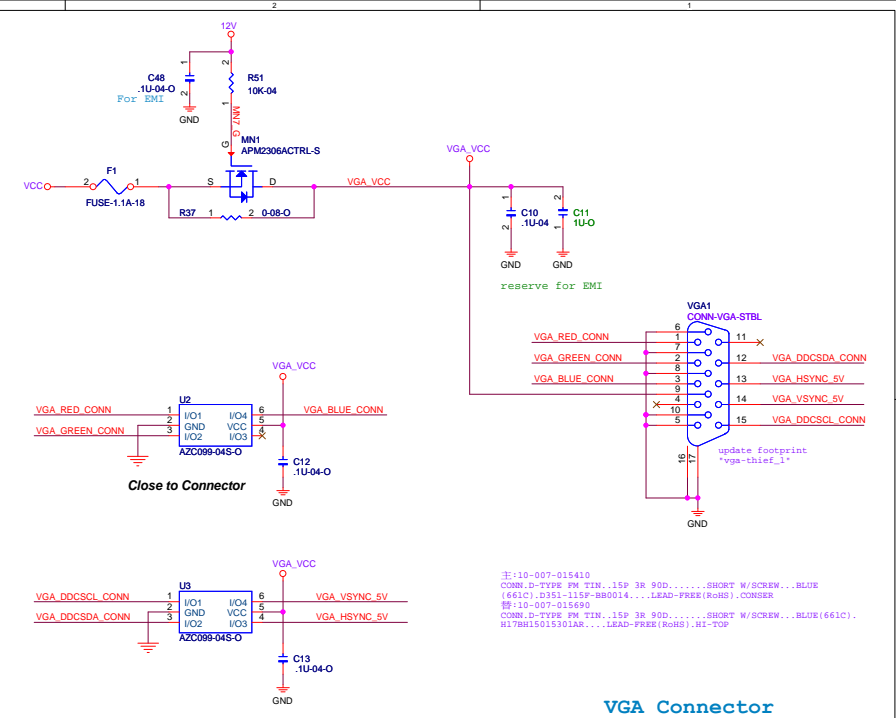
when stuff External EEPROM, pls check Demo 1 件



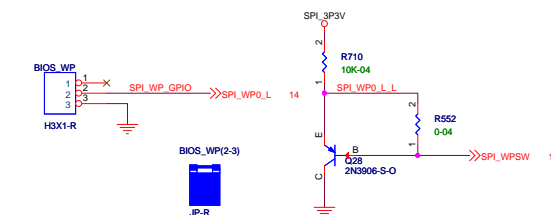
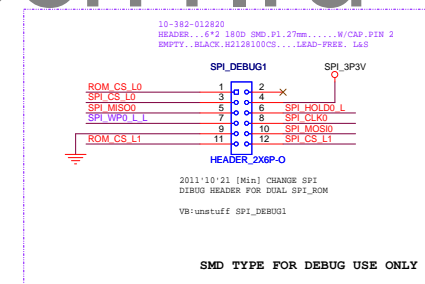
Elitegroup Computer Systems

File	LAN PHY - RTL8111E VL(B75)		
Size	Document Number	B75H2-AM-DNI	
C	Sheet	31	of 48
Date:	Wednesday, February 01, 2012		

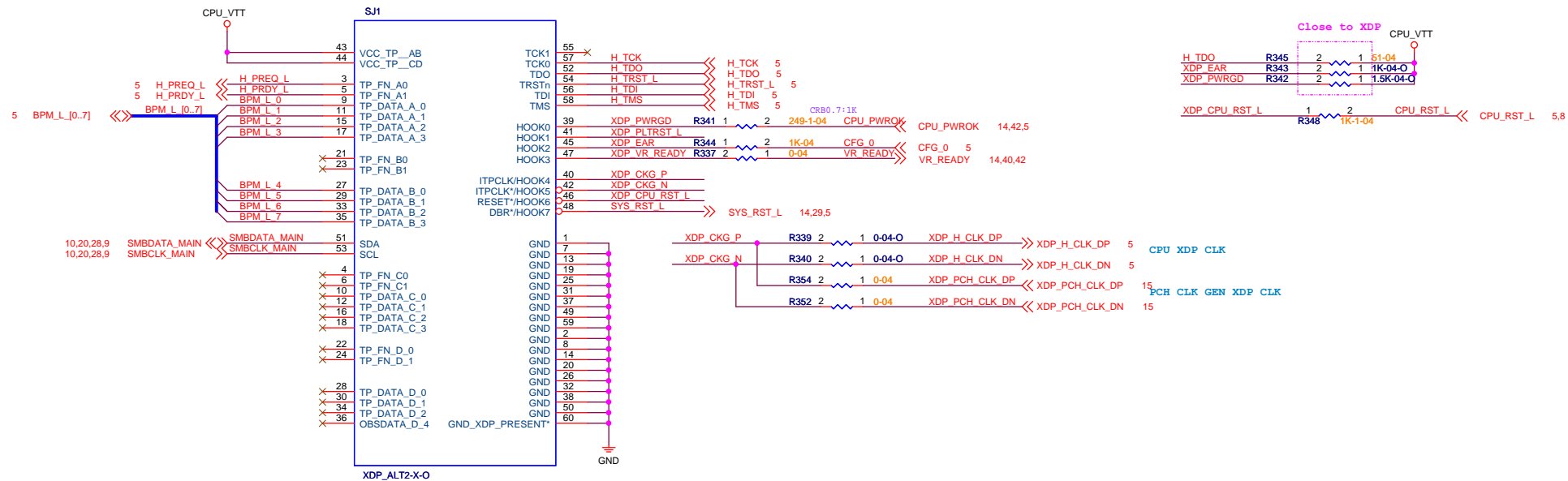




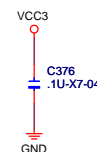
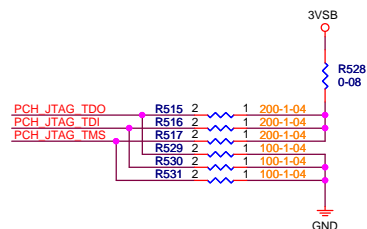
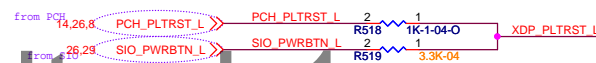
SPI ROM Circuit



BIOS WP Jumper:	
MODE	CLR CMO
BIOS WP	1-2
* NORMAL	2-3



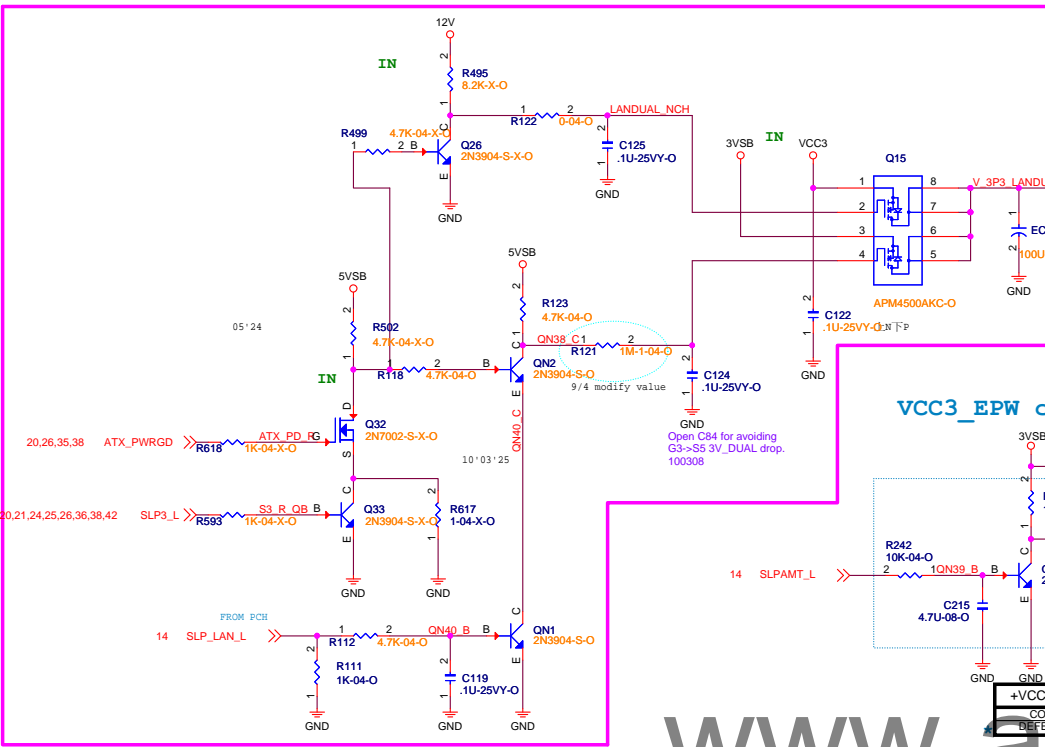
XDP Footprint:
 2x30_xdp_conn for Stuff XDP
 2x30_xdp_conn-nmnp for Reserve XDP



Stitching VIA 2011.10.05

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for B75 DEL SCH

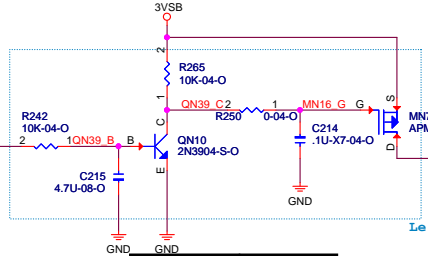


AMT 上件
NON AMT 上件

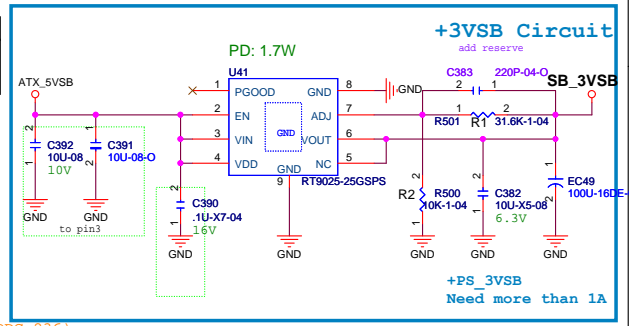
LAN Power Source	La	Lb	Lc
3V LANDUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN(NO WoL) or M0 Only	X	X	V

R97 for Q77,B75

VCC3_EPW control

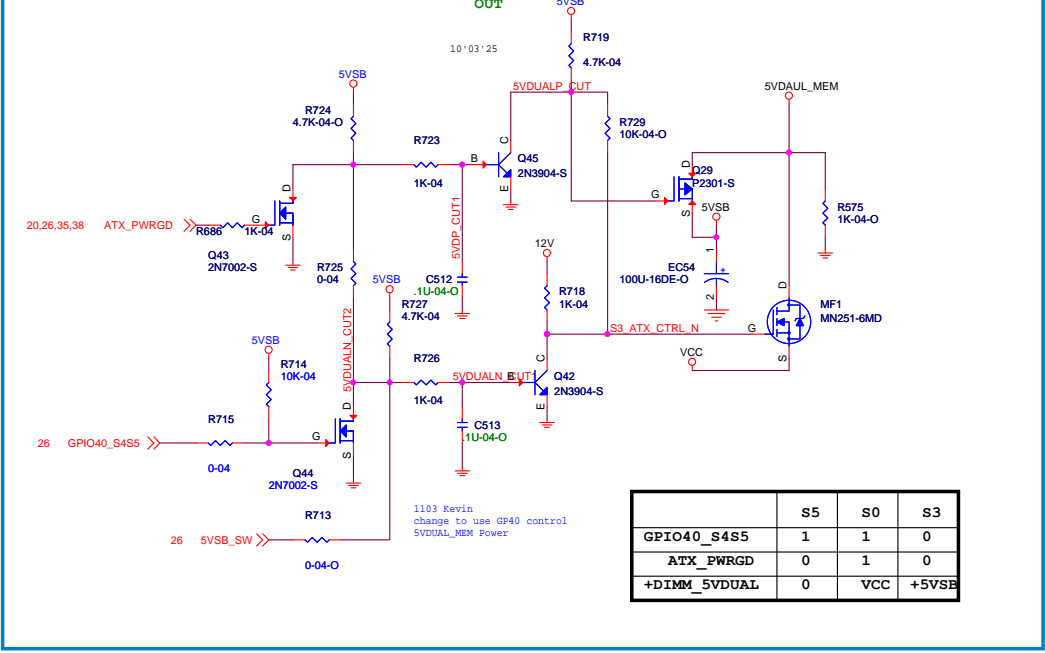


+VCC3_EPW	Ld	Le
COMBO	V	X
DEFENSIVE	X	V



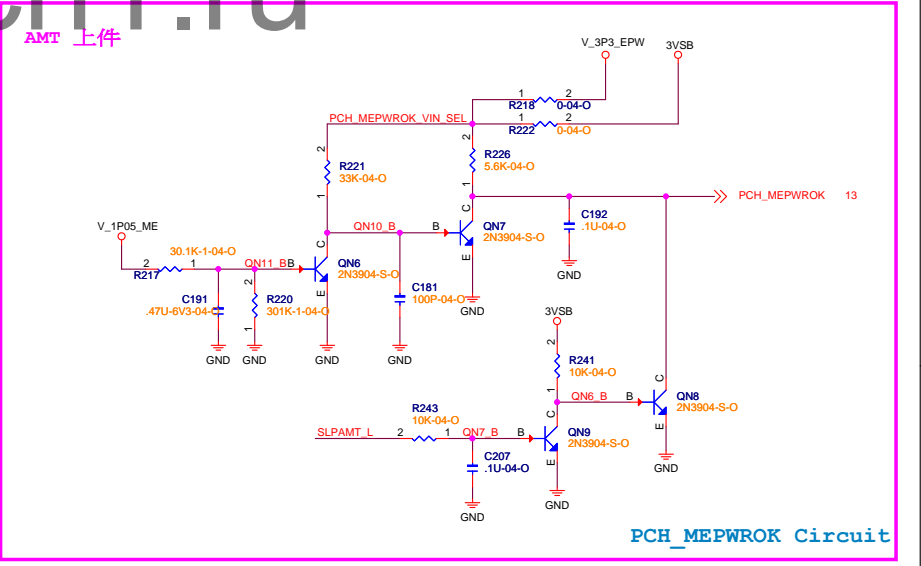
SR23 for H77

5VDUAL_MEM MODULE



	S5	S0	S3
GPIO40_S4S5	1	1	0
ATX_PWRGD	0	1	0
+DIMM_5VDUAL	0	VCC	+5VSB

for B75 DEL AMT SCH

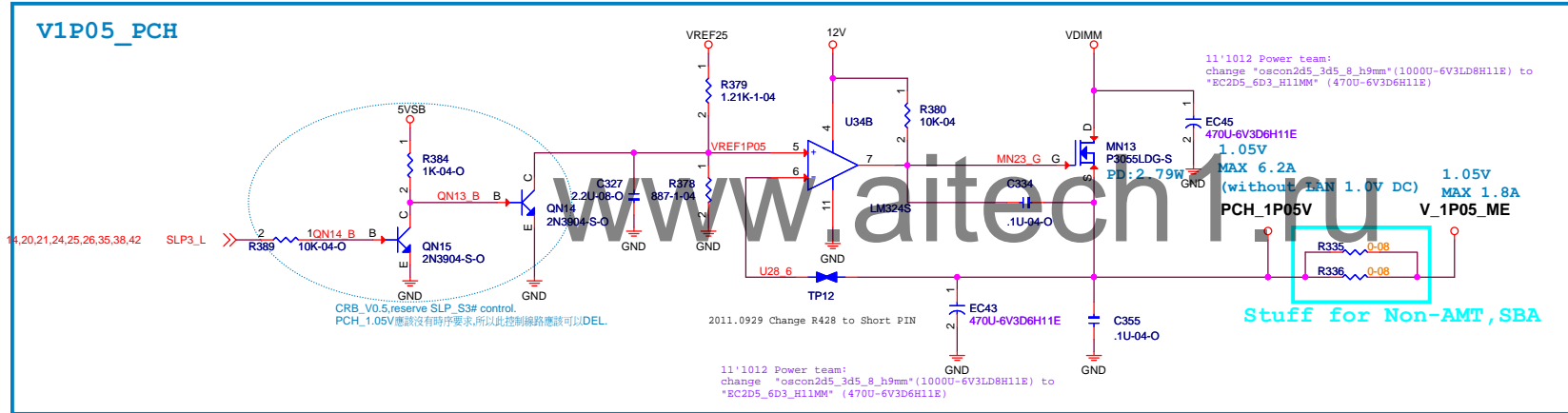


Elitegroup Computer Systems

Title: **DC/DC 3VSB/3VDUAL/5VDUAL**

Size: Custom
Document Number: **B75H2-AM-DNI**
Date: Wednesday, February 01, 2012
Sheet: 35 of 46

REMOVE ME POWER for Non-AMT, SBA

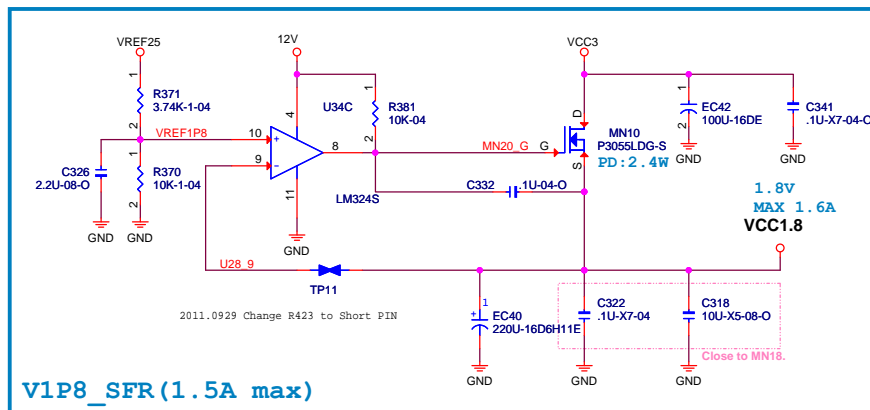
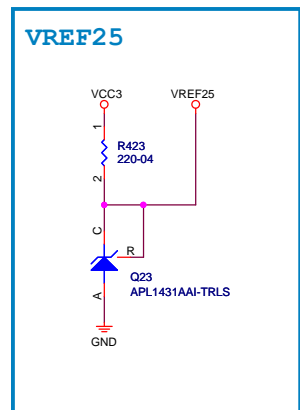
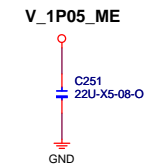


BOM Note:

02-340-015840....dfn10_r8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTEK

04-880-828100
C/C.8.2pF.50V.0.25pF..NPO....SMD 0402....LEAD-FREE(RoHS/HF).

05-152-240114
RES.240K.1/16W.1%..SMD 0402.....LEAD-FREE(RoHS/HF).



VDIMM

BOM Different

	Ra	Rb
RT8116A	9.1K	10nF
RT8120F	16K	3.3nF

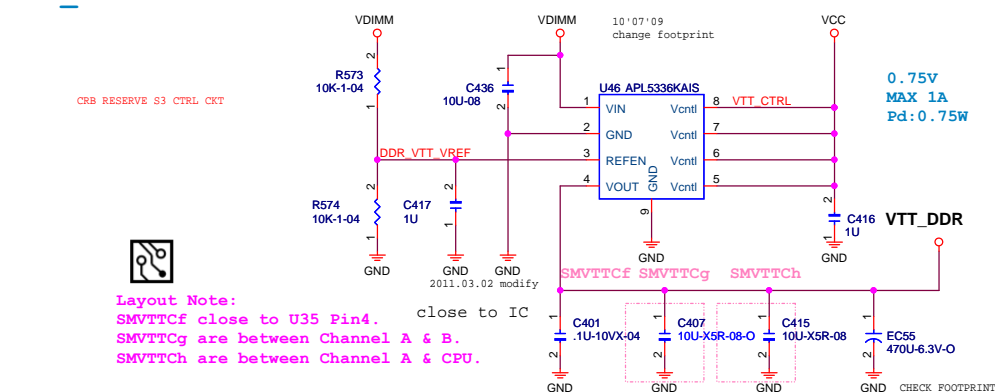
SLP4_L	High	Low
RT8120F	Enable	Disable

RT8120F & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-116790
IC PWM.RT8116AGS_SOP 8P.0.8V....LEAD-FREE
(Rohs(HF))RICHTEK
RT8120FGS
IC PWM.RT8120FGS_SOP 8P.0.8
V....HF.LEAD-FREE.RICHTEK

when the comp voltage is <0.4V, the RT8116 will be disable.
Double pole = 5.3KHz @1uH/820UF
Double pole = 4.0KHz @1uH/820UF*2
Double pole = 3.2KHz @1uH/820UF*3
Z1 = 2.27K @1.8K/0.39U SS=2.0mS
P1 = 157K @1.8K/560P

DDR_VTT

AP5336/GS9020/AME9172M



2011.0913 Modify footprint
for New Regulation

Layout Note:

EC43, EC49
Dual Value / Footprint:
560U-6V30D6H9E / OSCON2D5_6D3_H9MM
560U-6.3D-OS-J / EC3D5_8_H9MM_1P

1.5V
MAX 22A
OCP:36.7A

VDIMM

Layout Note:

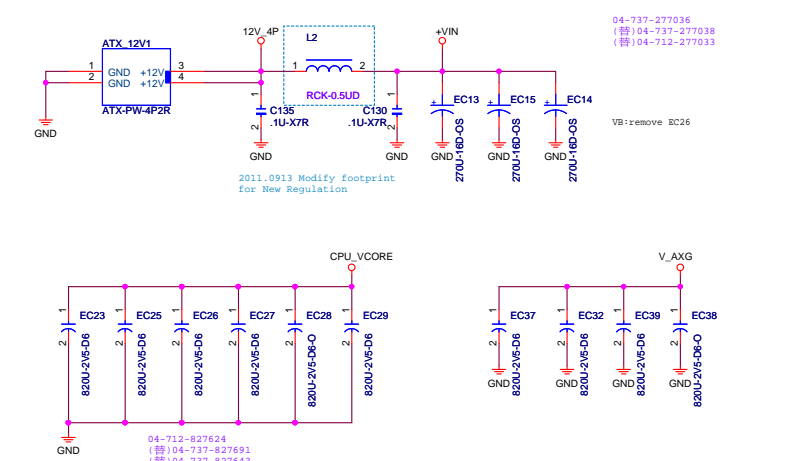
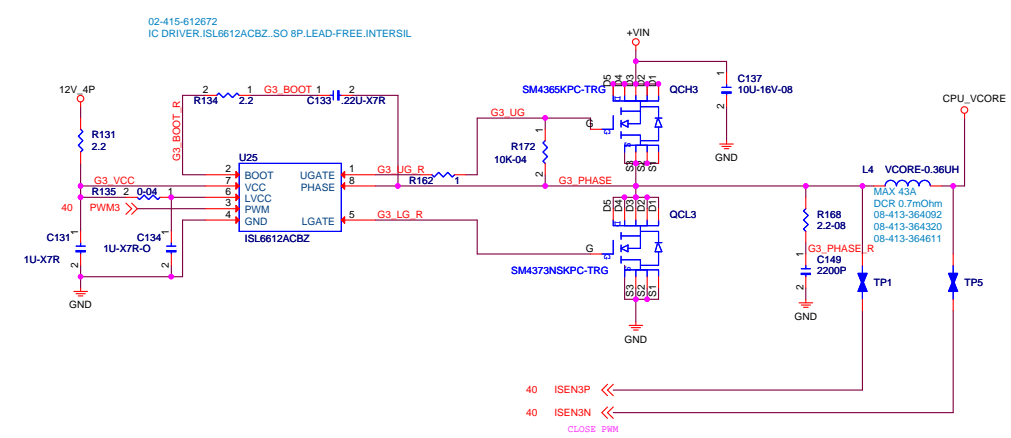
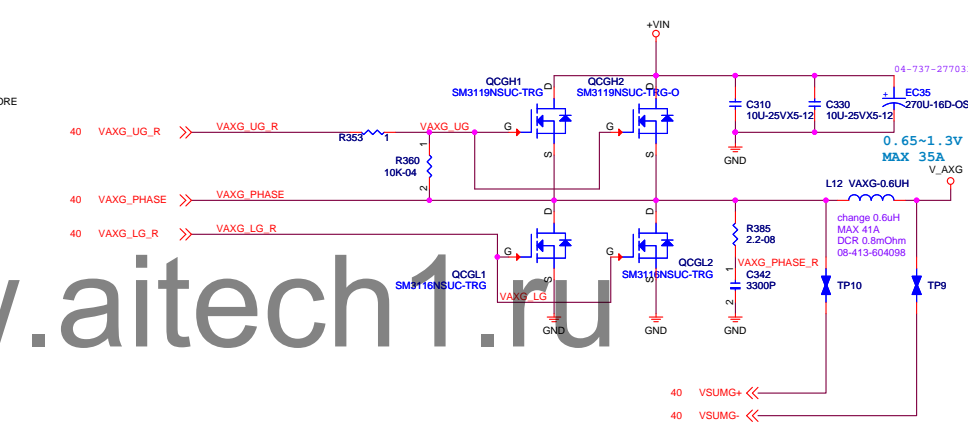
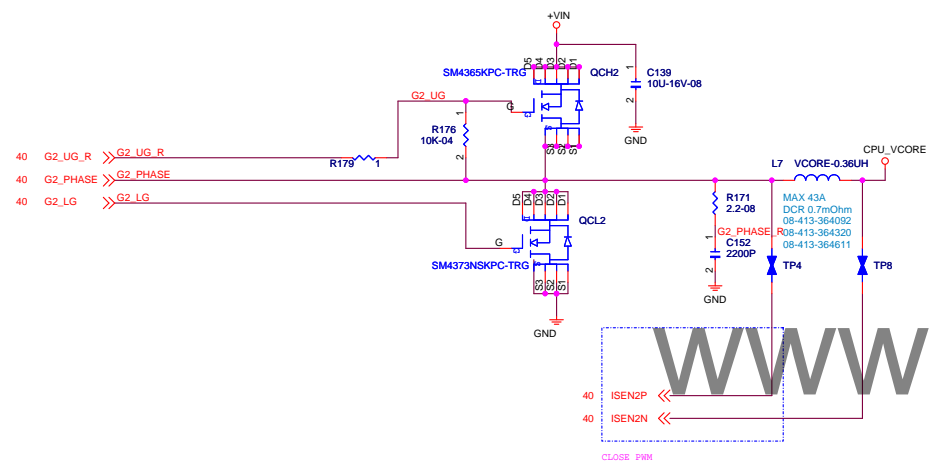
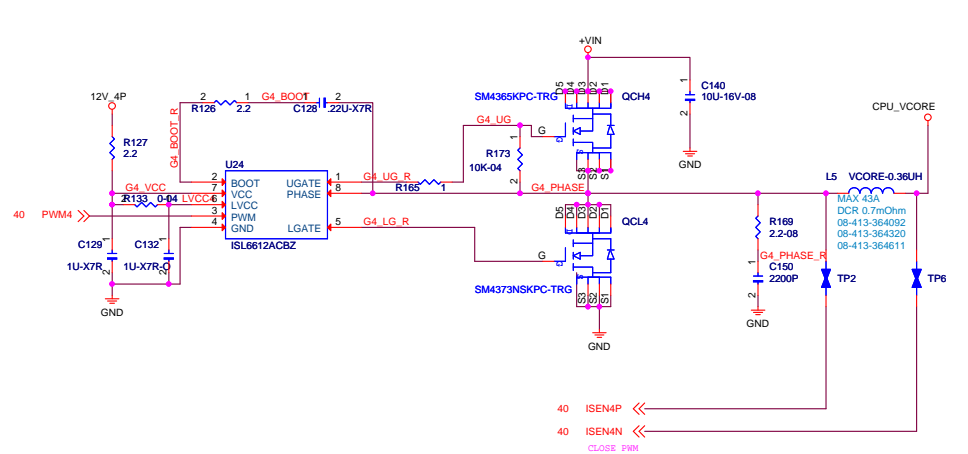
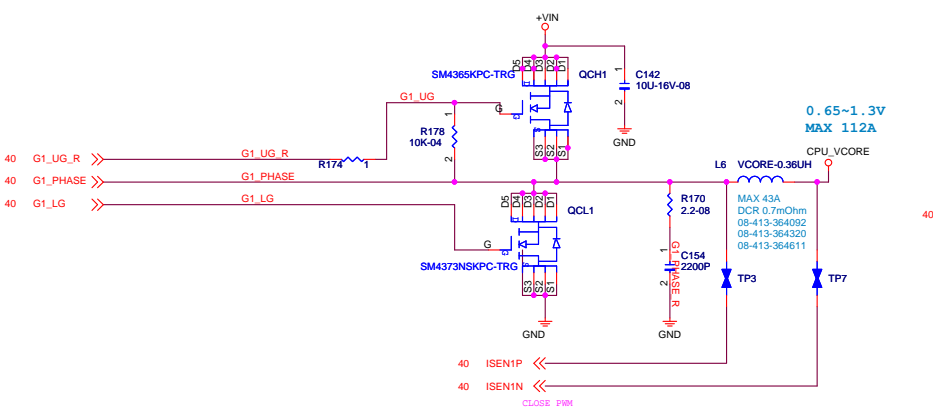
VSMCx are under Channel B.
VSMCy are between Channel A & B.
VSMCz are between Channel A & CPU.

Elitegroup Computer Systems

Title **DC/DC VDIMM/DDR_VTT**

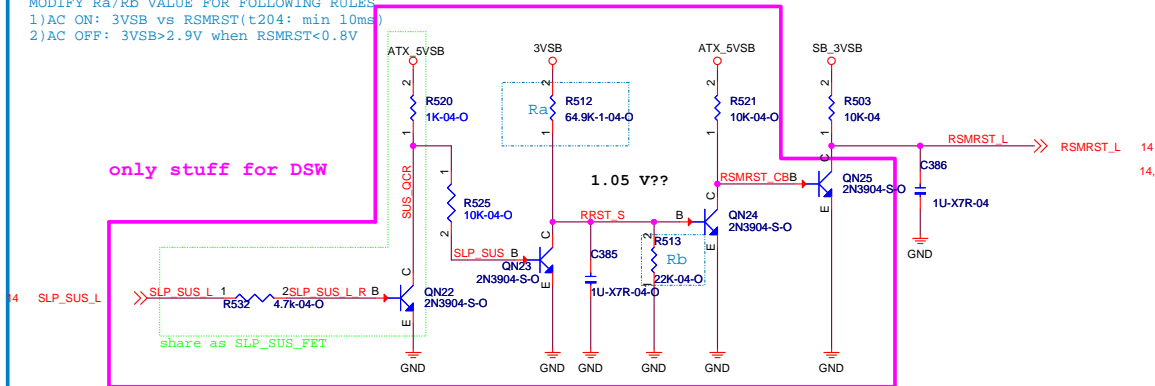
Size Custom Document Number **B75H2-AM-DNI** Rev A

Date: Thursday, February 02, 2012 Sheet 37 of 46

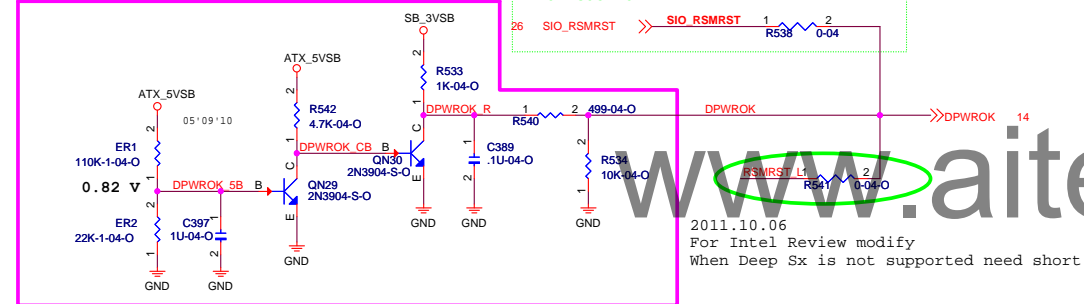


FOR DNI MODE DEL DSW 20120112

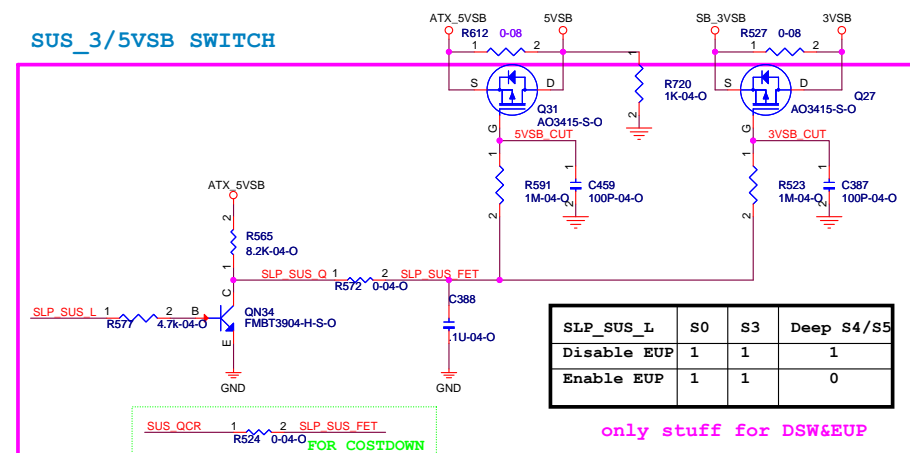
only stuff for DSW



FOR COSTDOWN

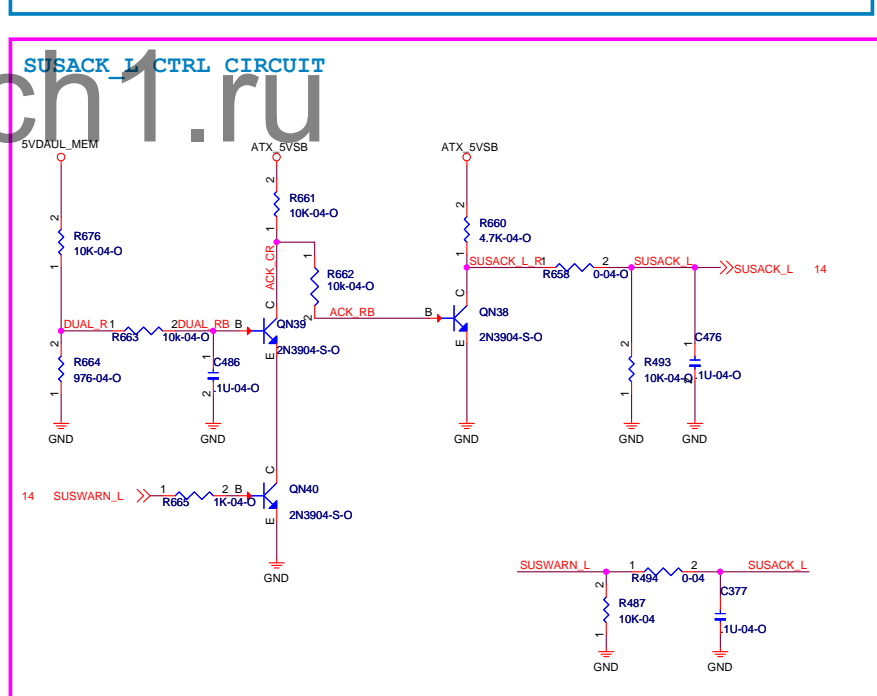


only stuff for DSW&EUP



SLP_SUS_L	S0	S3	Deep S4/S5
Disable EUP	1	1	1
Enable EUP	1	1	0

SUSACK_L CTRL CIRCUIT



Elitegroup Computer Systems

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ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching ISL6363 4+1 phases

Switching ISL95870B 1 phase

Switching NCP1587

DDR3 DIMM (2) 1333MHz	
VDDQ	15A_S0 1.0A_S3
V_SM_VTT	1.0A_S0

Linear LM324

LDO APL5336

Linear LM324

Intel Ivy Bridge CPU		
VCCP	V1D 0.25~1.52V	TDC :85A(95W)
VAXG	V1D 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.75A

Intel Panther Point (TDP 5.5W)		
V_PROC_IO	1.05V	2mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	2.52A
VccIO	1.05V	4.57A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.08A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.185A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.1A
VccSUS3_3	3.3V	0.01A
VccSUS3_3	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x1

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery 3V

B75

REALTEK RTL8111E_VL		
VDD3P3	3.3V	70mA
VDD1P0	1.0V	300mA
CTRL1P0 internal LVR Output		

LAN INTEL 82579		
VDD3P3	3.3V	90mA
VDD1P0	1V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8728 FX		
3VSB	3.3V	< 6mA (S0/S1/S3/S4/S5)
VCC3	3.3V	< 10mA (S0/S1)
BAT 3.3V	3.3V	<< 2 uA (S0/S1/S3/S4/S5)

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

LDO
12V 5V

www.aitech.ru

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

Total 2 Slots

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

Total 1 Slot

USB X4 Header	
VDD	5VDual
5VDual	2.0A

LAN/WAN

USB X4 IO	
VDD	5VDual
5VDual	2.0A

LAN/WAN

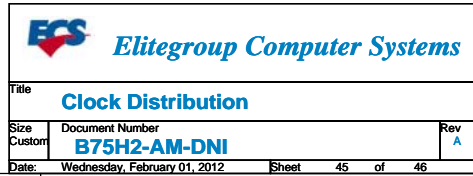
PS/2	
5VDual	1.0A

LAN/WAN

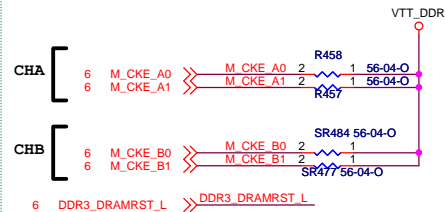
USB3.0X4 IO&Headers	
5VDUAL	3A

LAN/WAN

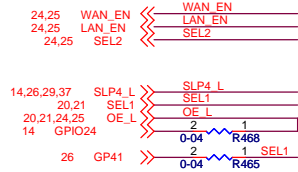
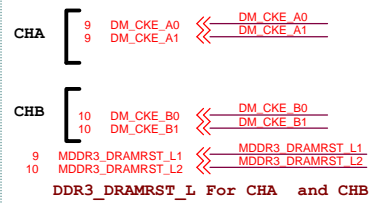
Maho Bay Platform has two clock mode:
 1. Integrated Clock Mode (Generate by PCH)
 2. Buffer Through Mode (Generate by Clock Gen.)
 If we choose Integrated Clock Mode, we should
 unstuff Clock Gen. circuit.
 Please refer to
 Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
 Page.13 PCH - SATA, SATA CONN for CLK IN PD
 Page.14 PCH - MISC, F/W Strap
 Page.15 PCH - CLK IO, CKG



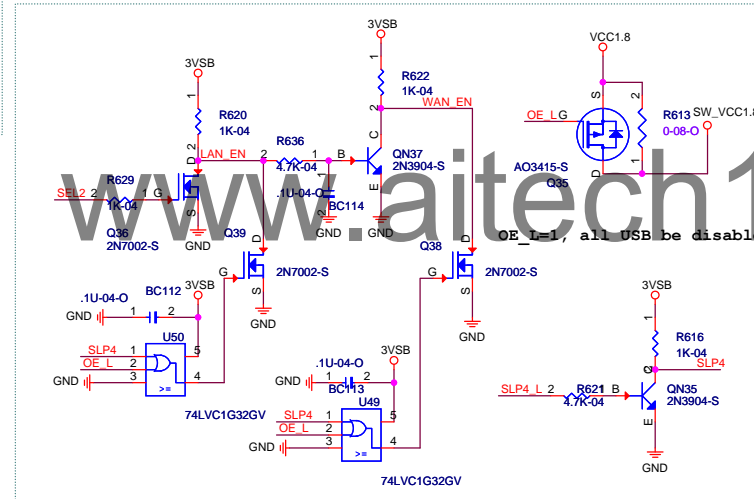
From CPU chip



output to dimm



SIO GP41 reversed for BIOS detect default setting 20111215
PCH GPIO24 as OE# GP in to confirm DUAL NET MODE



02-198-032130 IC TTL.
74LVC1G32GV..SOT-753-5
(SC-74A)...LEAD-FREE.NXP

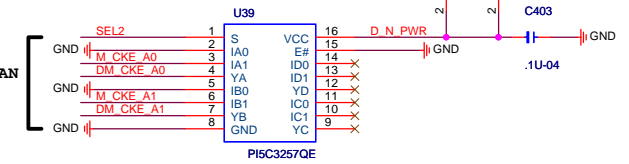
Y = A + B		
Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

SEL1 from PCI/PCIE slot SEL#

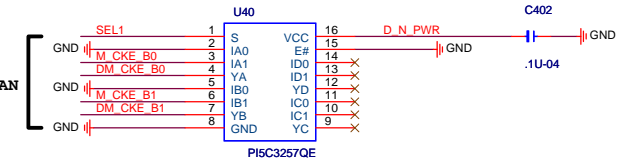
DUAL-NET MODE CONTROL SIGNAL

PCI SLOT	PCIEX1 SLOT	CONTROL SIGNAL
A9	A8	SLP_S3#
A11	A7	SEL#
B10	A5	PWRBTN#
B14	A6	OE#

CHA DIMM1 FOR WAN



CHB DIMM2 FOR LAN

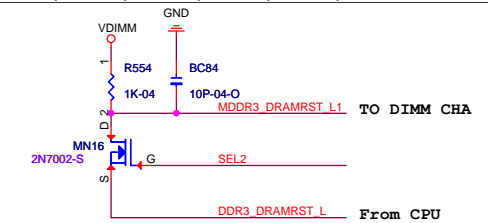


default setting SEL1=1, DIMM2 work, as LAN RAM

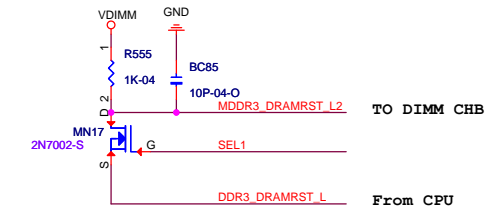
Truth Table⁽¹⁾

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

CHA DIMM1 FOR WAN



CHB DIMM2 FOR LAN



DUAL-NET MODE								
SEL	OE#							
	1	0	1	0	1	0	1	0
D_CKE_A0	link	open	link	open	link	open	link	open
D_CKE_A1	link	open	link	open	link	open	link	open
D_CKE_B0	link	open	link	open	link	open	link	open
D_CKE_B1	link	open	link	open	link	open	link	open
DDR3_DRAMRST_L1	link	open	link	open	link	open	link	open
DDR3_DRAMRST_L2	link	open	link	open	link	open	link	open

★